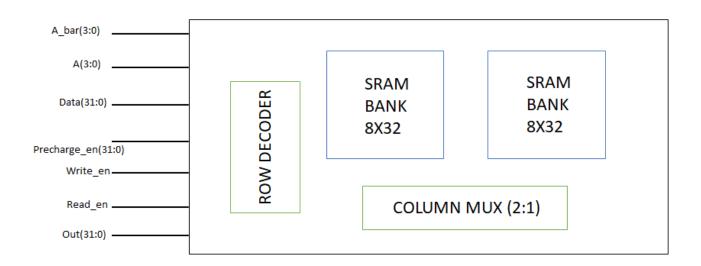
# EE 577A- Fall 2021 VLSI SYSTEM DESIGN

Lab2 Report 512-bit SRAM Array Design

> Ti-Shen Chueh tchueh@usc.edu 3751474091

In this lab, we will design a 512-bit SRAM with two 256-bit banks. The word length is 16 bits.



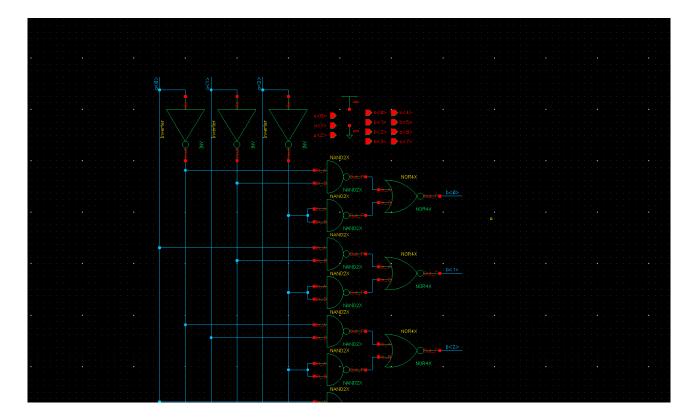
Below is the summary of the input pins:

INPUT	ADDRESS BITS	A[3]-A[0], <u>A_bar[</u> 3]- <u>A_bar[</u> 0]	Transition time =5ps
INPUT	READ CONTROL	<u>Read_en</u>	Transition time =5ps
INPUT	WRITE CONTROL	<u>Write_en</u>	Transition time =5ps
INPUT	PRECHARGE CONTROL	Precharge_en	Transition time =5ps
INPUT	WRITE DATA BITS	Data[31]-data[0]	Transition time =5ps
INPUT	READ DATA BITS	Out[31]-out[0]	Transition time =5ps

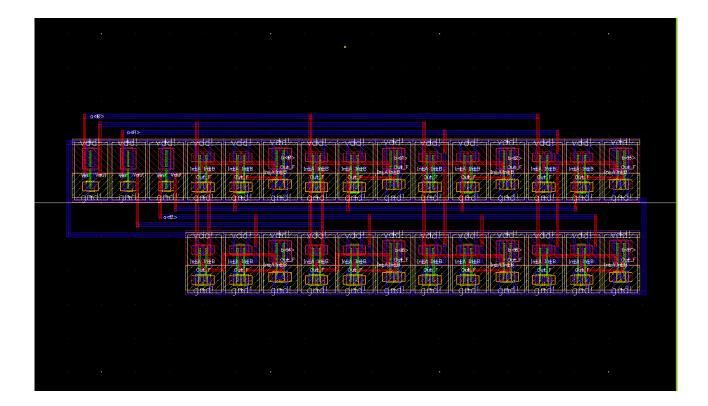
# 3-8 Decoder (Schematic)

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The figure below is the pre-decode system for 3-8 decoder.

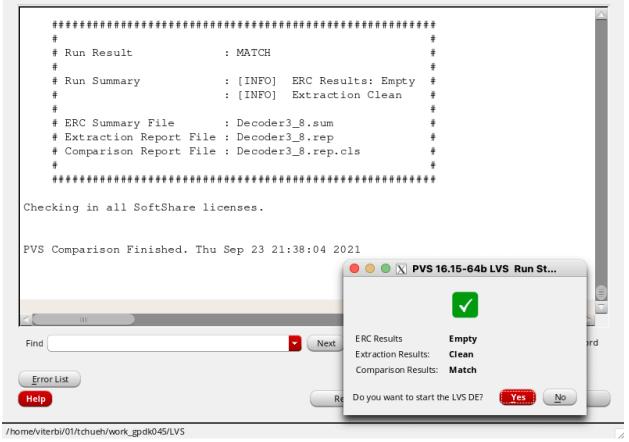


### 3-8 Decoder (Layout)



Time       : 1 (s)         Used       : 30 (M)         nal Geometry       : 264 (3101)         uleChecks       : 562         esults       : 0 (0)         be found in file Decoder3_8.sum         Voltage       VS 16.15-64b DRC Results Viewer         v Options Tools Windows Help       cādence         Voltage       : :::::::::::::::::::::::::::::::::::	Total CPU Time : 1 (s) Total Real Time : 1 (s) Peak Memory Used : 30 (M) Total Original Geometry : 264 (3101) Total DRC RuleChecks : 562 Total DRC Results : 0 (0) Summary can be found in file Decoder3_8.sum ASCI Check File View Options Tools Windows Help cadence File View Options Tools Windows Help cadence Desi Cells Compared to the file of t	Total CPU Time       : 1 (s)         Total Real Time       : 1 (s)         Peak Memory Used       : 30 (M)         Total Original Geometry       : 264 (3101)         Total DRC RuleChecks       : 562         Total DRC Results       : 0 (0)         Summary can be found in file Decoder3_8.sum         ASCI       Image: Cadence         File View Options Tools Windows Help       Cadence         Desi       Image: Cells       Image: Rules         Image: Cell/Rule       Hier       Top       Cells       Rules         Show: Image: Cells       Image: Rules       Show: Image: Cells       Show: Image: Cells       Image: Rules	Total CPU Time       : 1 (s)         Total Real Time       : 1 (s)         Peak Memory Used       : 30 (M)         Total Original Geometry       : 264 (3101)         Total DRC RuleChecks       : 562         Total DRC Results       : 0 (0)         Summary can be found in file Decoder3_8.sum       ASCI         Sched       Results Viewer         File View Options Tools Windows Help       cādence         Desi       Cells       ? Show: @ O & @ & 1
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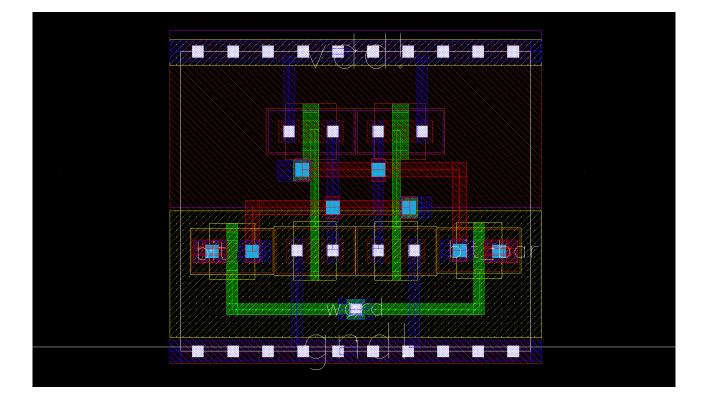
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#### SRAM Cell (Schematic)

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# SRAM Cell (Layout)



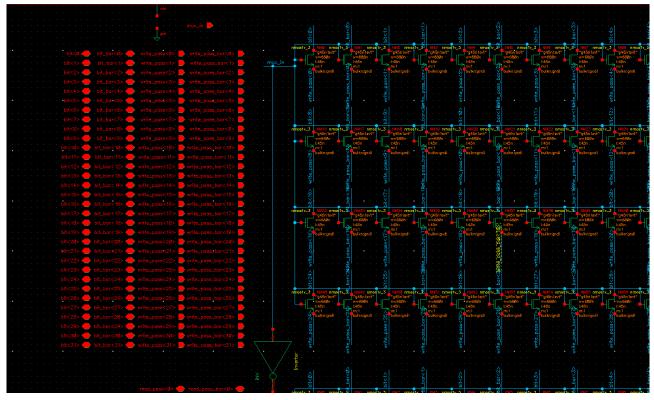
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[LVS] LVS × [DRC] DRC ×	
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PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)	
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)	
Total CPU Time : 1(s)	
Total Real Time : 1(s)	
Peak Memory Used : 26(M)	
Total Original Geometry : 123(193)	
Total DRC RuleChecks : 562	
Total DRC Results : 0 (0)	
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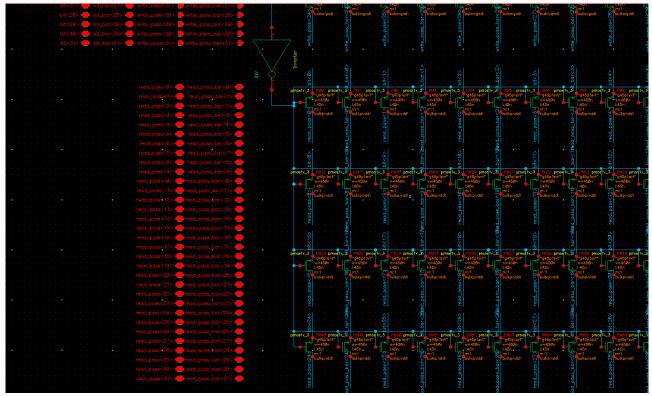
### Write/Read MUX (Schematic)

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The figure below shows that nMOS pass transistors ( W = 680nm / L = 45nm) is used to design the column write MUX.

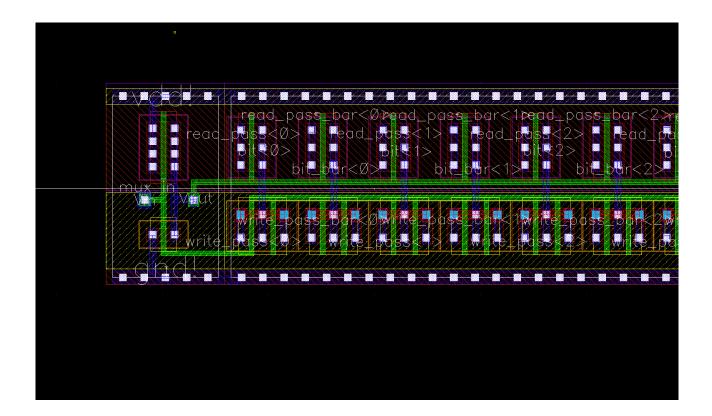


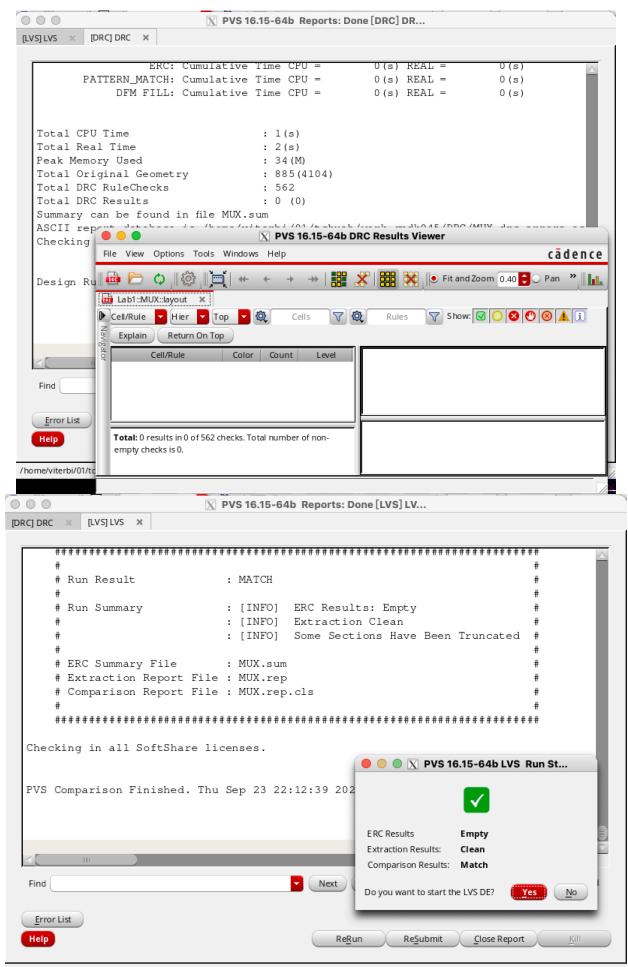
The figure below shows that pMOS pass transistors ( W = 450nm / L = 45nm) is used to design the column read MUX.



### Write/Read MUX (Layout)

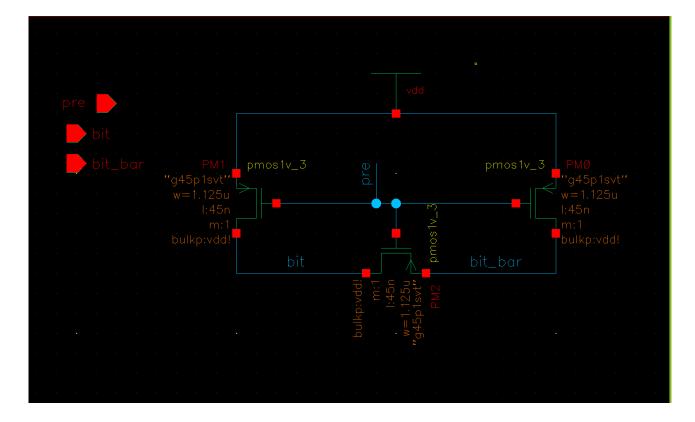
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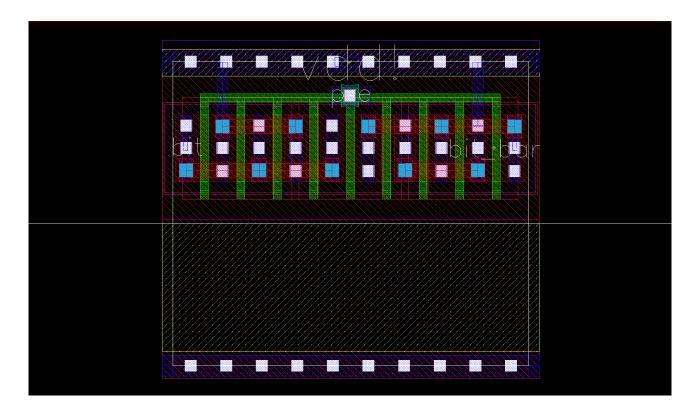


<sup>/</sup>home/viterbi/01/tchueh/work\_gpdk045/LVS

### Pre-charge (Schematic)



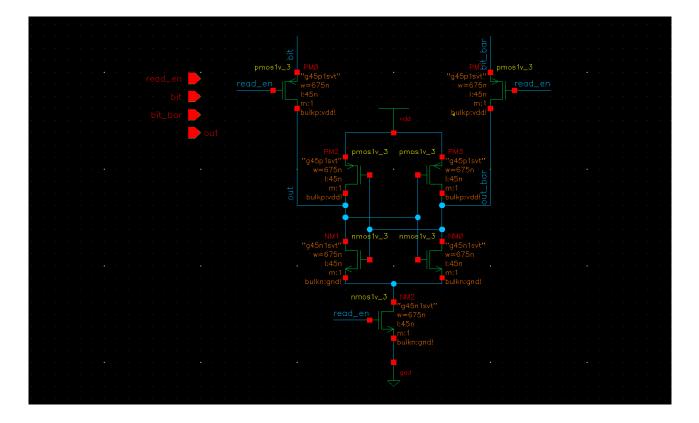
#### Pre-charge (Layout)



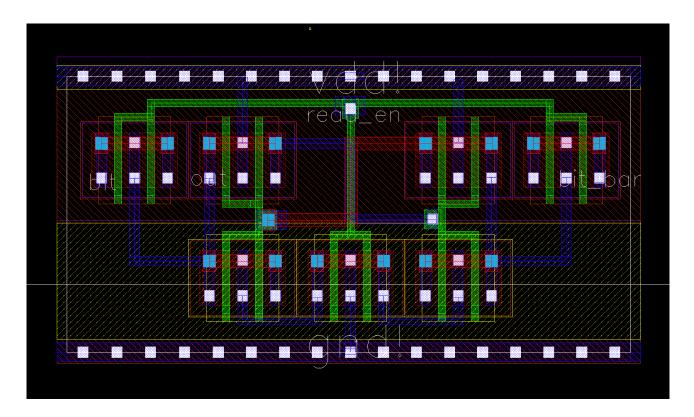
000 X PVS 16.15-64b Reports: Done [DRC] DR... [LVS] LVS × [DRC] DRC × ERC: Cumulative Time CPU = 0(s) REAL = 0(s)PATTERN\_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s) DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s) Total CPU Time : 1(s) Total Real Time : 1(s) Peak Memory Used : 26(M) Total Original Geometry : 93(202) Total DRC RuleChecks : 562 Total DRC Results : 0 (0) Summary can be found in file PrechargeCell.sum ASCI O PVS 16.15-64b DRC Results Viewer Checl File View Options Tools Windows Help cādence 📠 🎦 🗘 🔯 🏋 🔶 + + + + 🙀 💽 Fit and Zoom 0.40 💭 Pan 🔌 📊 Desi 📠 Lab1::PrechargeCell::layout 🛛 🗙 💎 Show: 🔽 🔿 🔇 🕐 🔕 🛕 🗓 🕨 Cell/Rule 🧧 Hier 🔽 Top 🔽 🥸 70 Rules Cells Explain (Return On Top ugato Cell/Rule Color Count Level Find Error Total: 0 results in 0 of 562 checks. Total number of nonempty checks is 0. Help /home/viter 000 X PVS 16.15-64b Reports: Done [LVS] LV... [DRC] DRC × [LVS] LVS × \*\*\*\*\*\*\* # Run Result : MATCH # : [INFO] ERC Results: Empty # Run Summary : [INFO] Extraction Clean # ERC Summary File : PrechargeCell.sum # Extraction Report File : PrechargeCell.rep # Comparison Report File : PrechargeCell.rep.cls \*\*\*\*\*\* Checking in all SoftShare licenses. 🛑 🔵 🔘 📉 PVS 16.15-64b LVS Run St... PVS Comparison Finished. Thu Sep 23 21:44:20 2021 ERC Results Empty Extraction Results: Clean Comparison Results: Match Find Next Pre Do you want to start the LVS DE? Yes No Error List Help ReRun ReSubmit Close Report

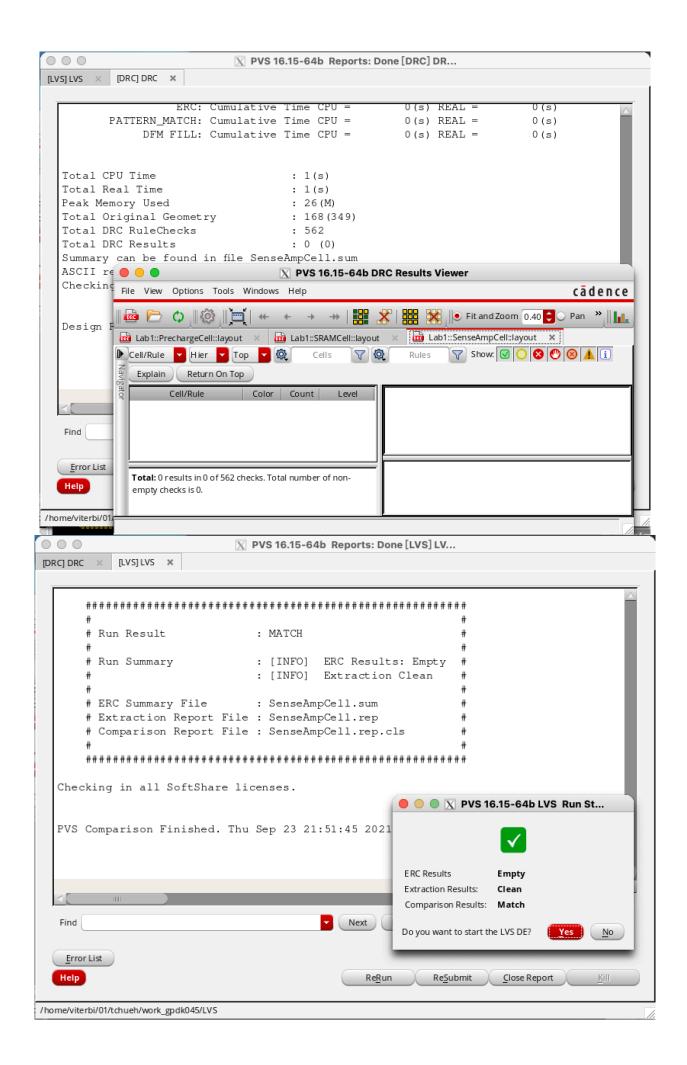
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### Sense Amp. (Schematic)

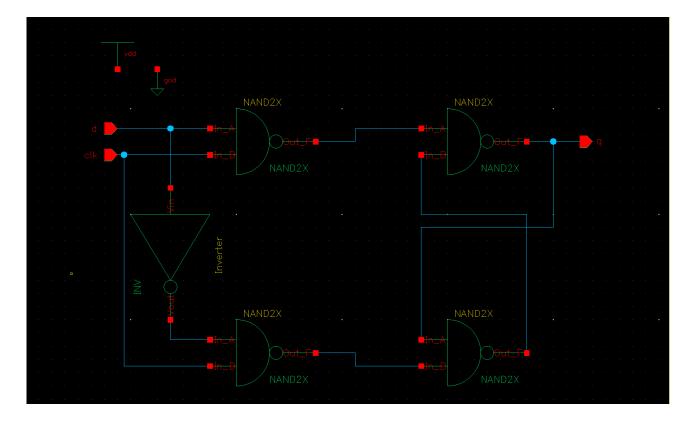


Sense Amp. (Layout)



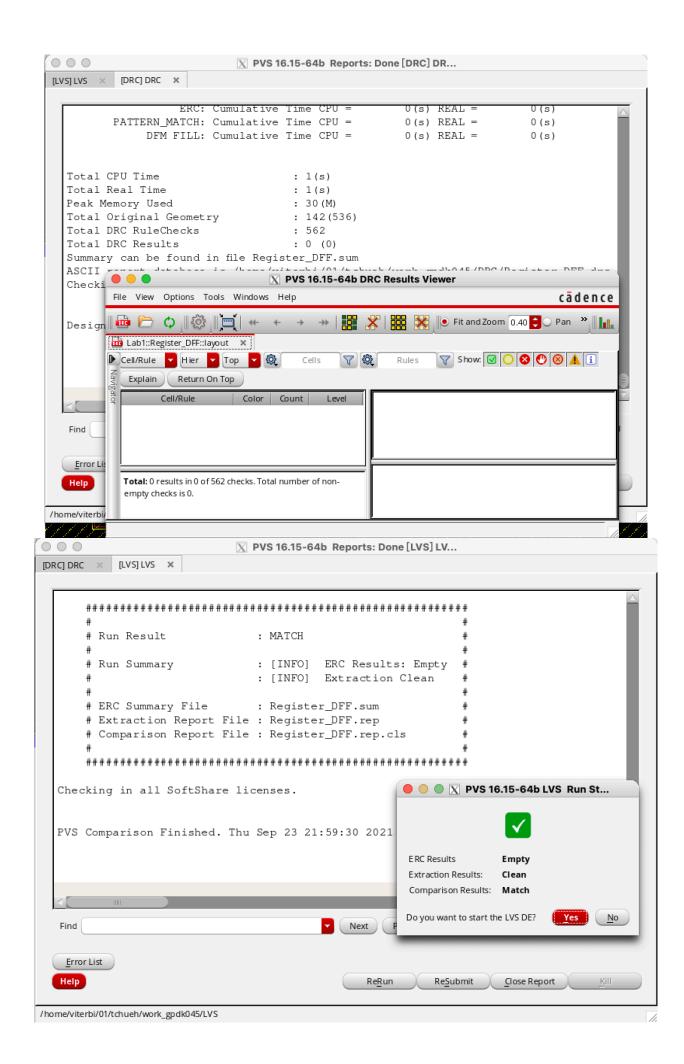


# Register (Schematic)

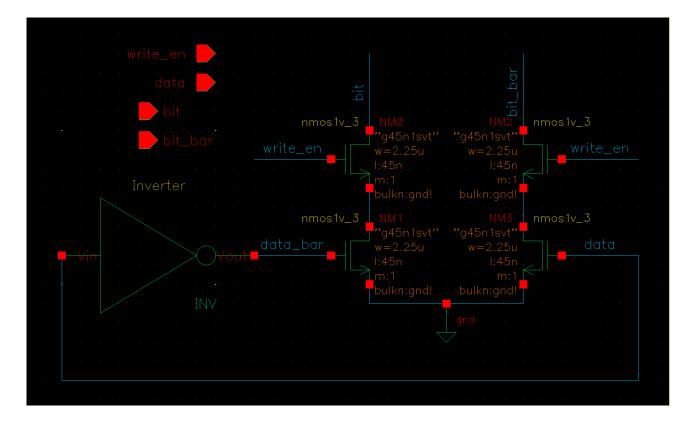


### Register (Layout)

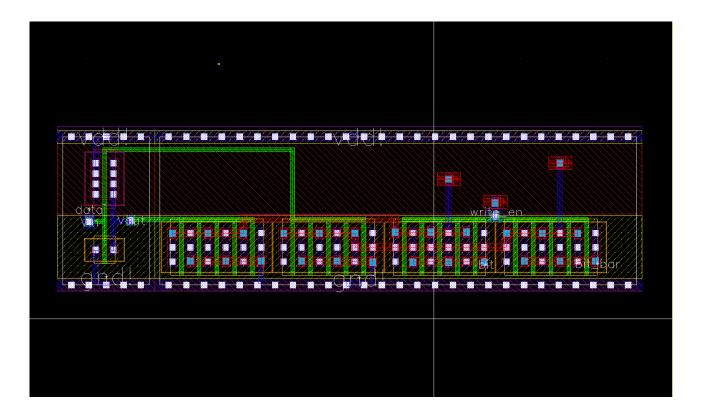
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Write Path (Schematic)



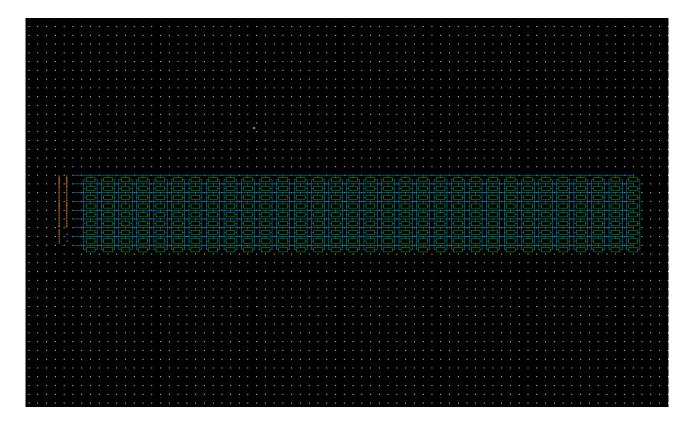
Write Path (Layout)



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[LVS] LVS × [DRC] DRC ×
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s) DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used     : 30 (M)       Total Original Geometry     : 255 (525)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
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Help Total: 0 results in 0 of 562 checks. Total number of non- empty checks is 0.
/home/viterbi/01/
Vertical State     VS 16.15-64b     Reports: Done [LVS] LV
$[DRC] DRC \times [LVS] LVS \times$
# # Run Result : MATCH #
# #
<pre># Run Summary : [INFO] ERC Results: Empty # # : [INFO] Extraction Clean #</pre>
# #
<pre># ERC Summary File : WritePathCell.sum # # Extraction Report File : WritePathCell.rep #</pre>
# Comparison Report File : WritePathCell.rep.cls #
# #
*****
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 21:56:10 20:
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Find Next Do you want to start the LVS DE? Yes No d
<u>Error List</u>
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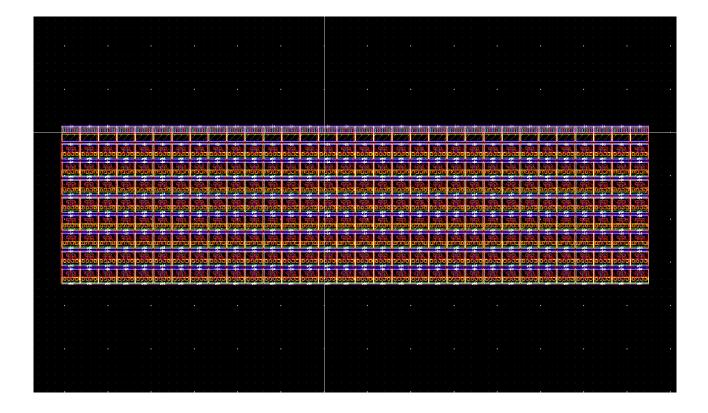
#### SRAM 8x32 Bank (Schematic)



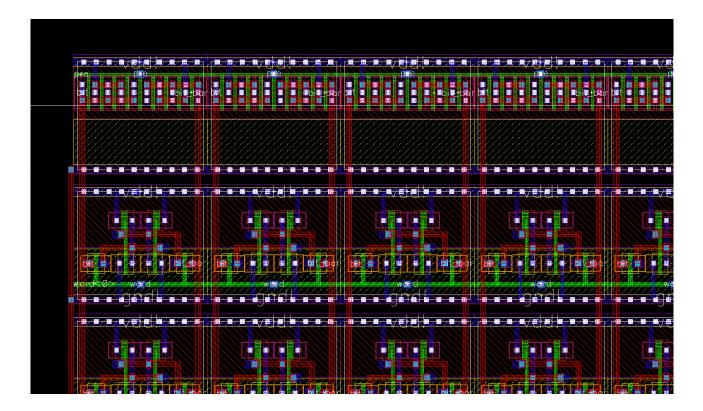
Each 256-bit SRAM bank was constructed with 8 row, 32 columns. The pre-charge was placed at the first row and connected to all the bit line and bit line bars.

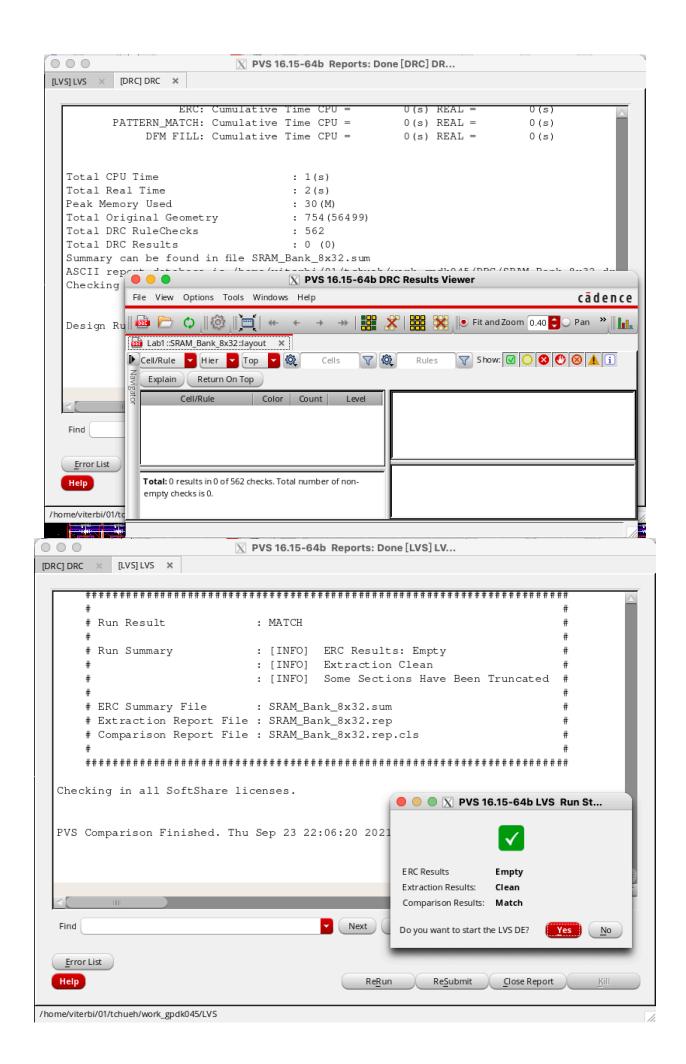
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#### SRAM 8x32 Bank (Layout)



The first row is the pre-charge system and following with 8 SRAM Cells.

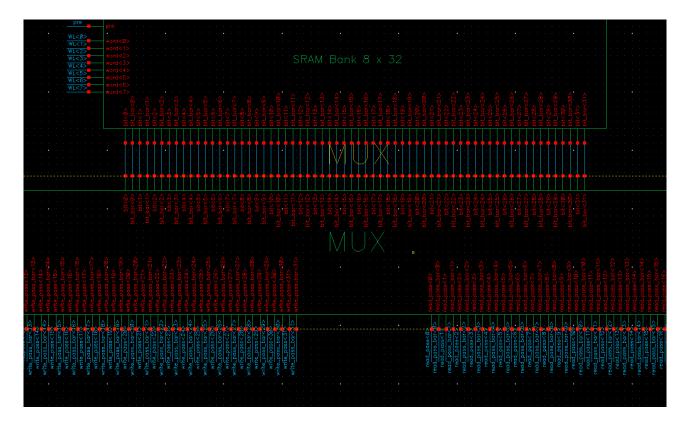


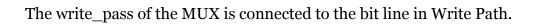


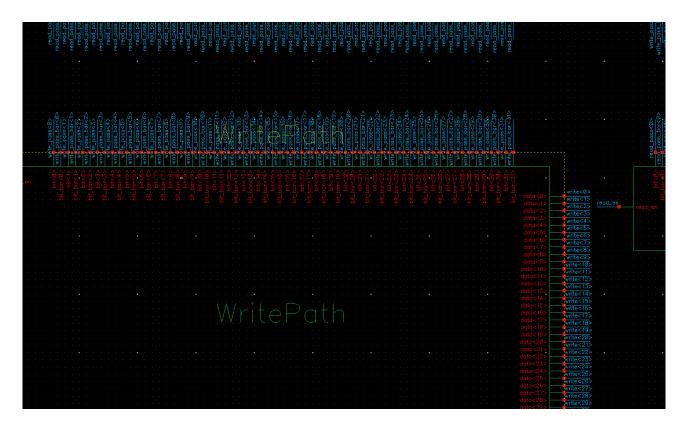
### SRAM 512-bit (Schematic)

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The SRAM Bank is connected to write/read MUX.







The read\_pass of the MUX is connected to the bit line in Sense Amp.

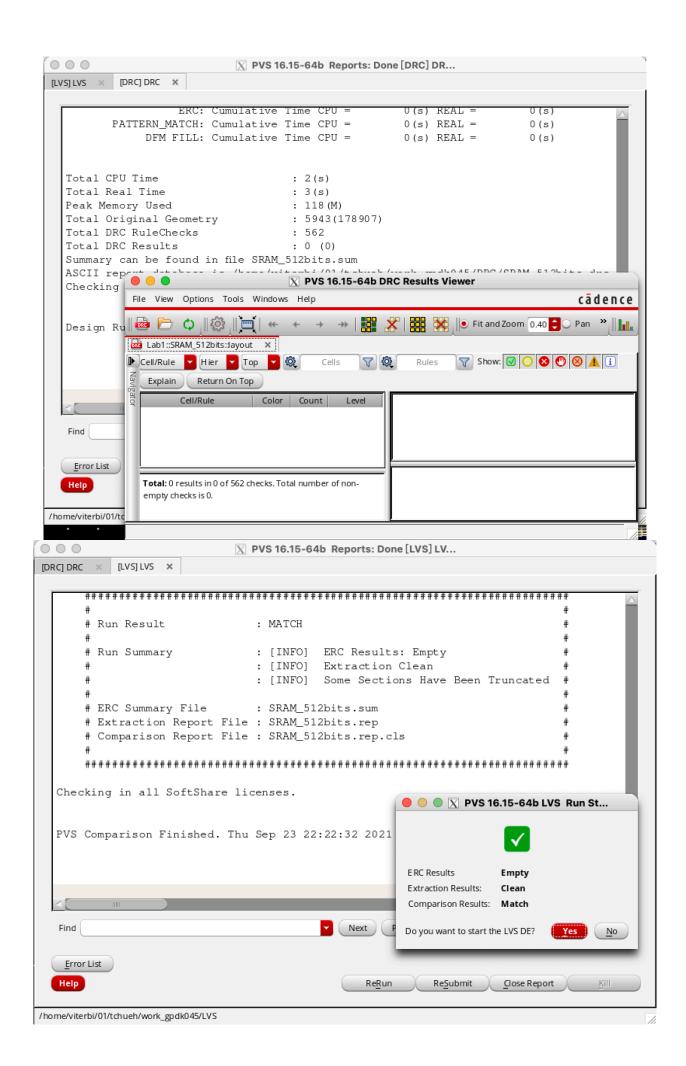
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The figure below is the I/O pins of the SRAM 512-bit.

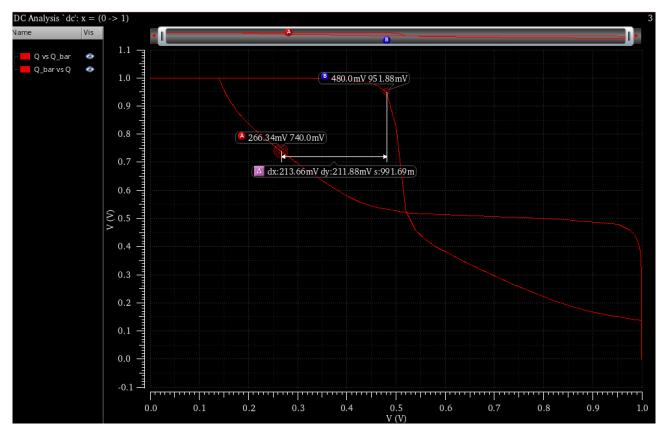
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	addr<3> 📂	write<7> 📂	write<23> 📄	<b>out</b> <7>	<b>out</b> <23> •	<u>WL&lt;7&gt;</u>
		write<8> 🕨	write<24>	out<8>	out<24>	
		write<9>	1			
		write<9>	write<25>	out<9>	out<25>	
		write<10> 📂	write<26>	🗩 out<10>	<b>out</b> <26>	
		write<11> 📄	write<27> 📂	🚽 📄 out<11>	<b>b</b> out<27>	
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### SRAM 512-bit (Layout)

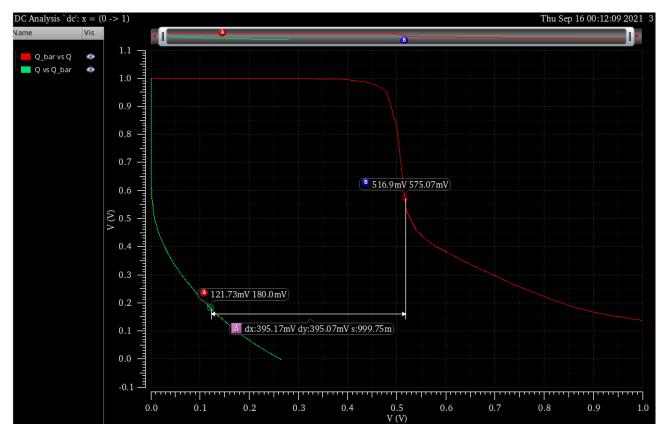
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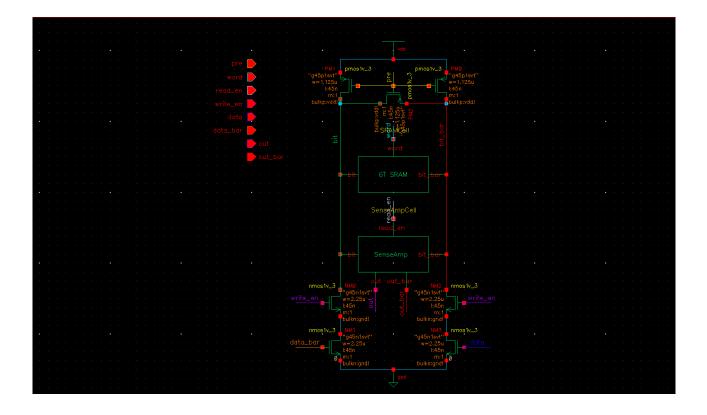
#### Read SNM is at least 190mV



#### Write SNM is at least 395mV



#### SRAM One Cell (Schematic)



The figure below shows the simulation for the single SRAM Cell with the waveform of the operation Write  $1 \rightarrow \text{Read} \rightarrow 1 \rightarrow \text{Write } 0 \rightarrow \text{Read} 0$ .



Write 1Read 1Write 0Read 012.57 ps8.52 ps11.49 ps8.52 ps

SRAM operation:

During the write operation, the 32-bit input data will be send to the Write Path. The addr<3> is going decide which Memory Bank will save the data. After that, the output of the Write Path (bit / bit\_bar) is pass through the nMOS pass transistors in the MUX and stored in the 256-bit SRAM Bank.

During the read operation, the address we got will decide which word line and which Memory Bank to read from. The Sense Amplifier sense the difference in the bit and bit\_bar when the pMOS pass transistors in the MUX tuns on.

Register at the output controls the information when it is available at the clock edge as the Sense Amplifier sense the difference.

Summary:

Area 173.325 x 38.807 = 6726.22328  $\mu m^2$ 

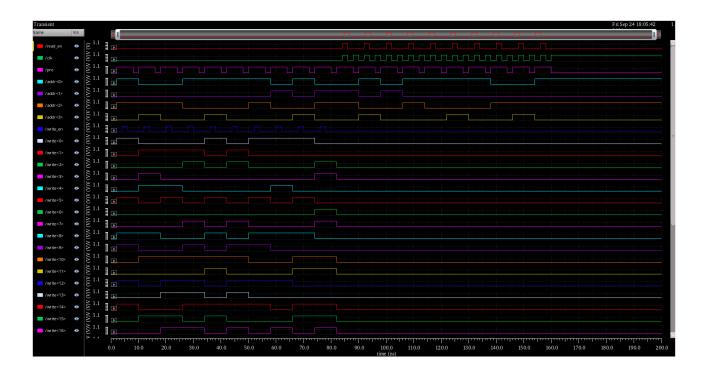
Complete time: 160 ns

Clock Frequency: 1/4 ns = 250 MHz

Read 10 data values (32 bit each) from a vector file and write into the SRAM in a sequential order starting from the last digit of your USC ID and then read 10 of them in the sequence of your USC ID.

SEQUENCE	A[3]-A[0]	DATA[31]-[0]
0	0100	143B B432
1	0101	2134 5321
2	0111	ABCD 1234
3	0110	2231 CCCC
4	0001	3211 7686
5	0010	ABCD 1111
6	1000	12AB CD91
7	1001	1296 CD21
8	1010	7A5A 6531
9	1100	6432 851A

### SRAM 512-bit (Schematic Waveform)

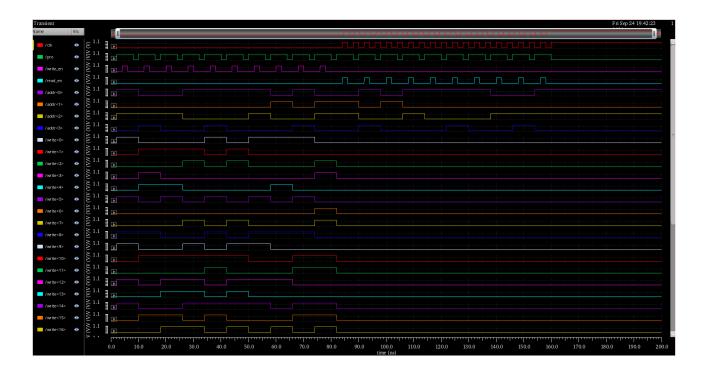


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	0		10.0	20.0	30.0	40.0	50.0	00.0	70.0	50.0	90.0	100.0 time (ns)	110.0	120.0	130.0	140.0	150.0	100.0	1/0.0	180.0	190.0

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### SRAM 512-bit (Extracted Waveform)



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