EE 577A- Fall 2021 VLSI SYSTEM DESIGN

Lab2 Report

512-bit SRAM Array Design

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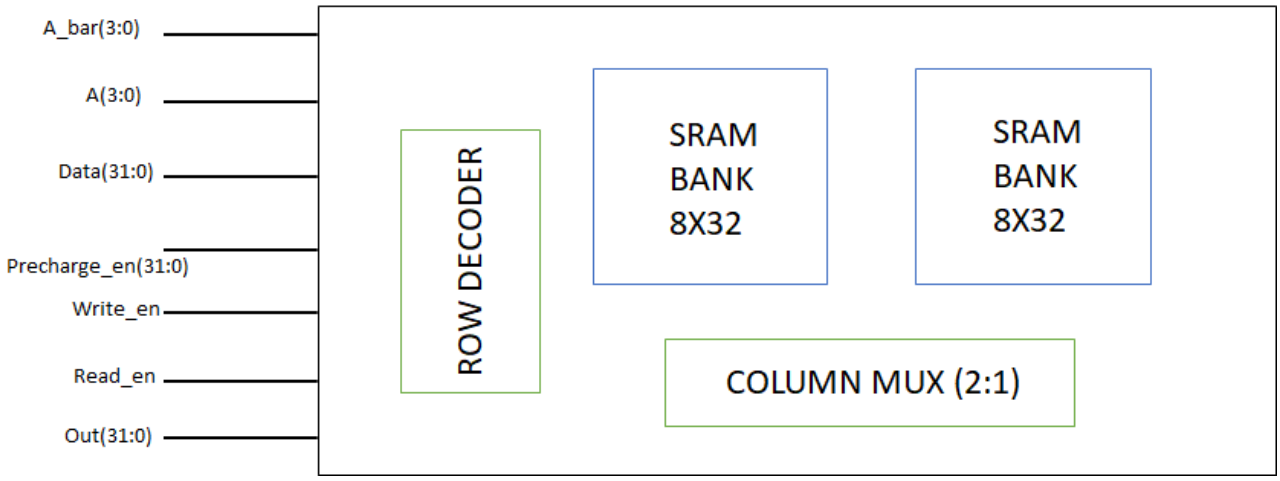
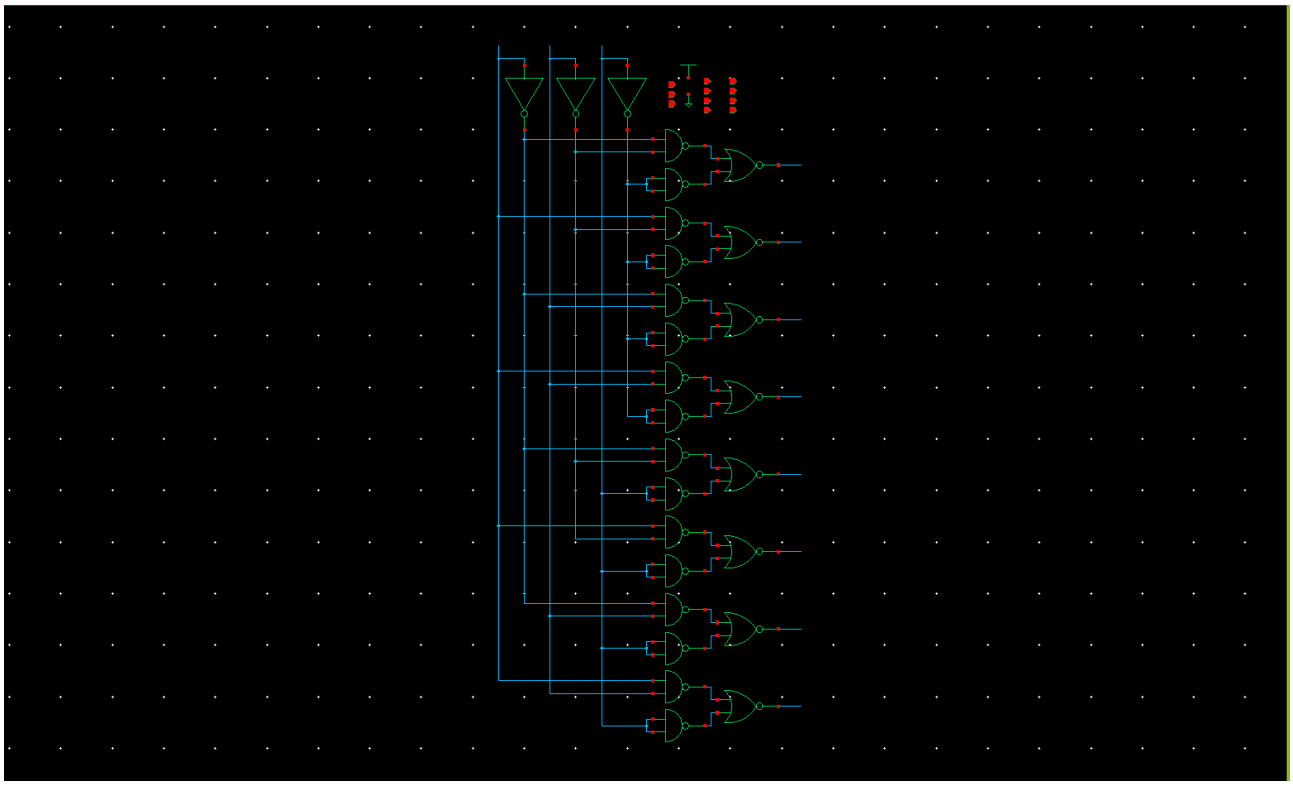
In this lab, we will design a 512-bit SRAM with two 256-bit banks. The word length is 16 bits.



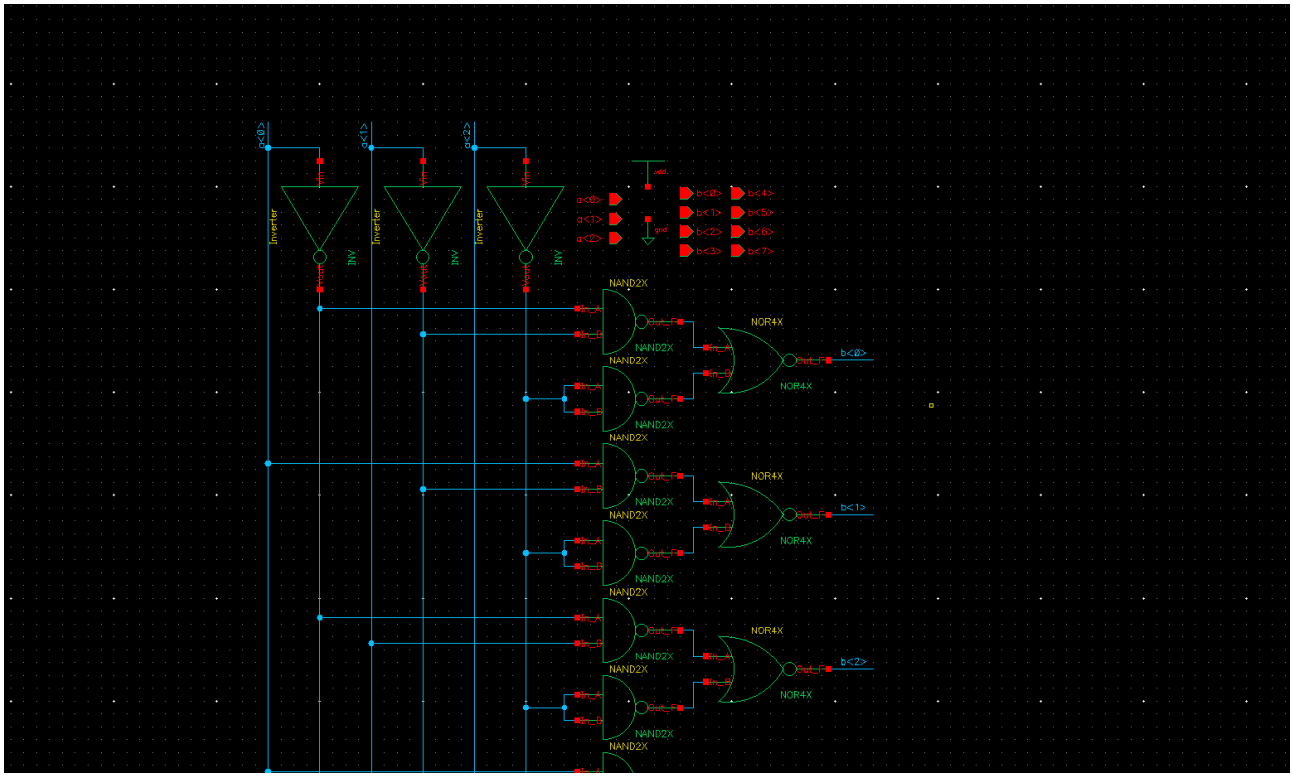
Below is the summary of the input pins:

INPUT	ADDRESS BITS	A[3]-A[0],A_bar[3]-A_bar[0]	Transition time =5ps
INPUT	READ CONTROL	Read_en	Transition time =5ps
INPUT	WRITE CONTROL	Write_en	Transition time =5ps
INPUT	PRECHARGE CONTROL	Precharge_en	Transition time =5ps
INPUT	WRITE DATA BITS	Data[31]-data[0]	Transition time =5ps
INPUT	READ DATA BITS	Out[31]-out[0]	Transition time =5ps

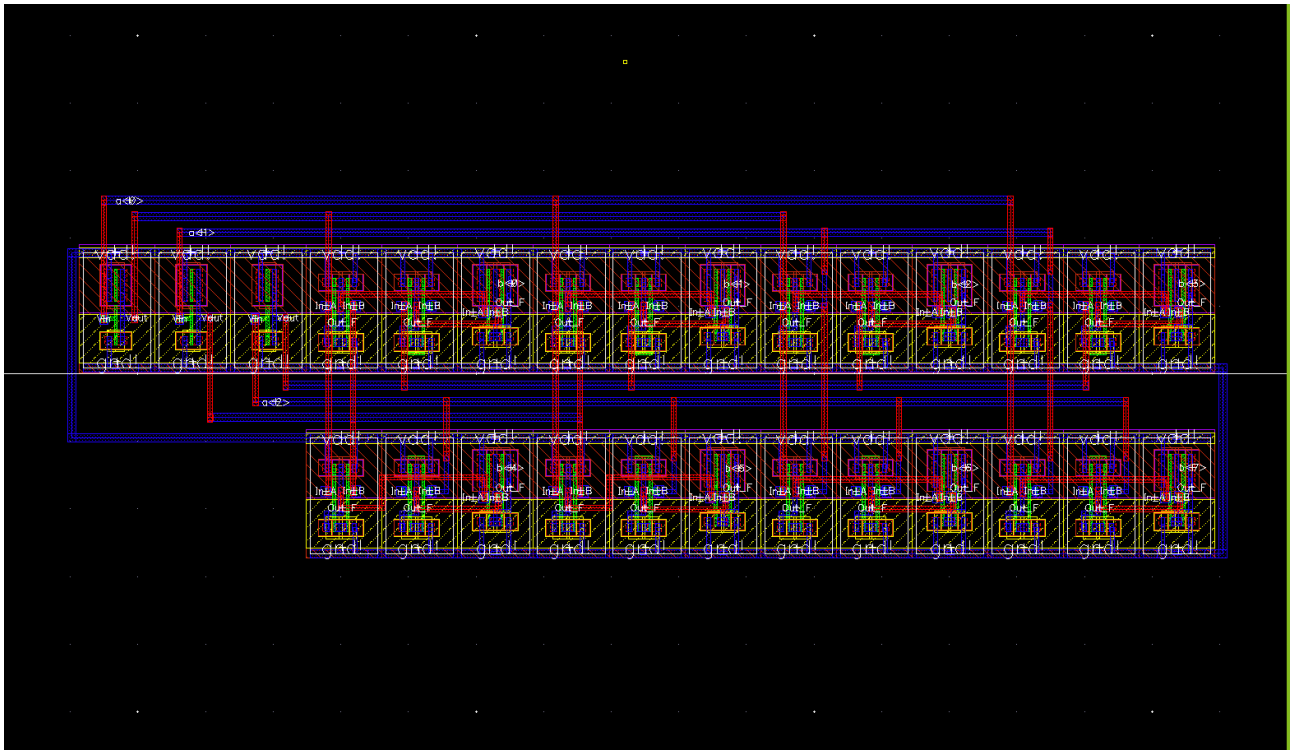
3-8 Decoder (Schematic)

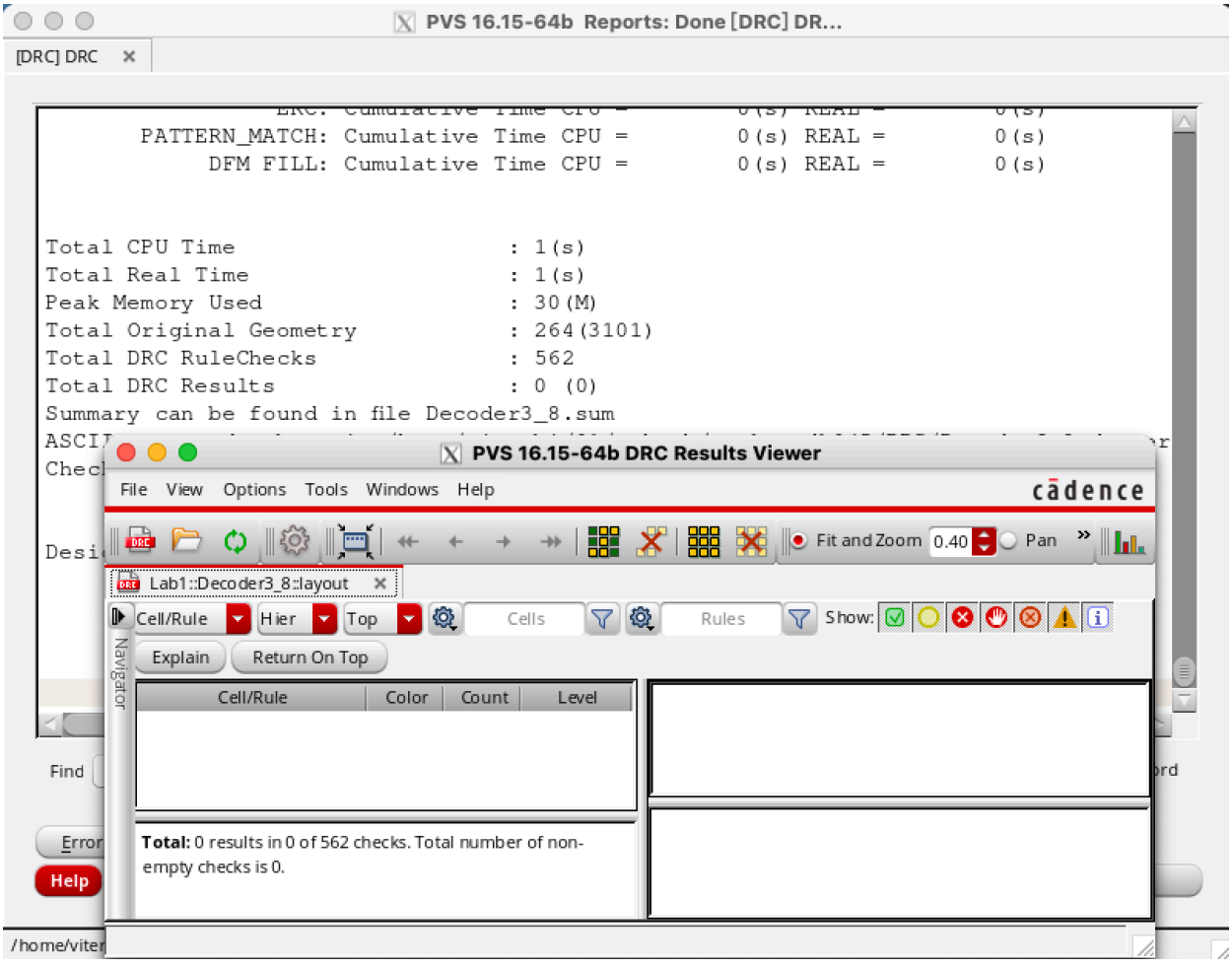


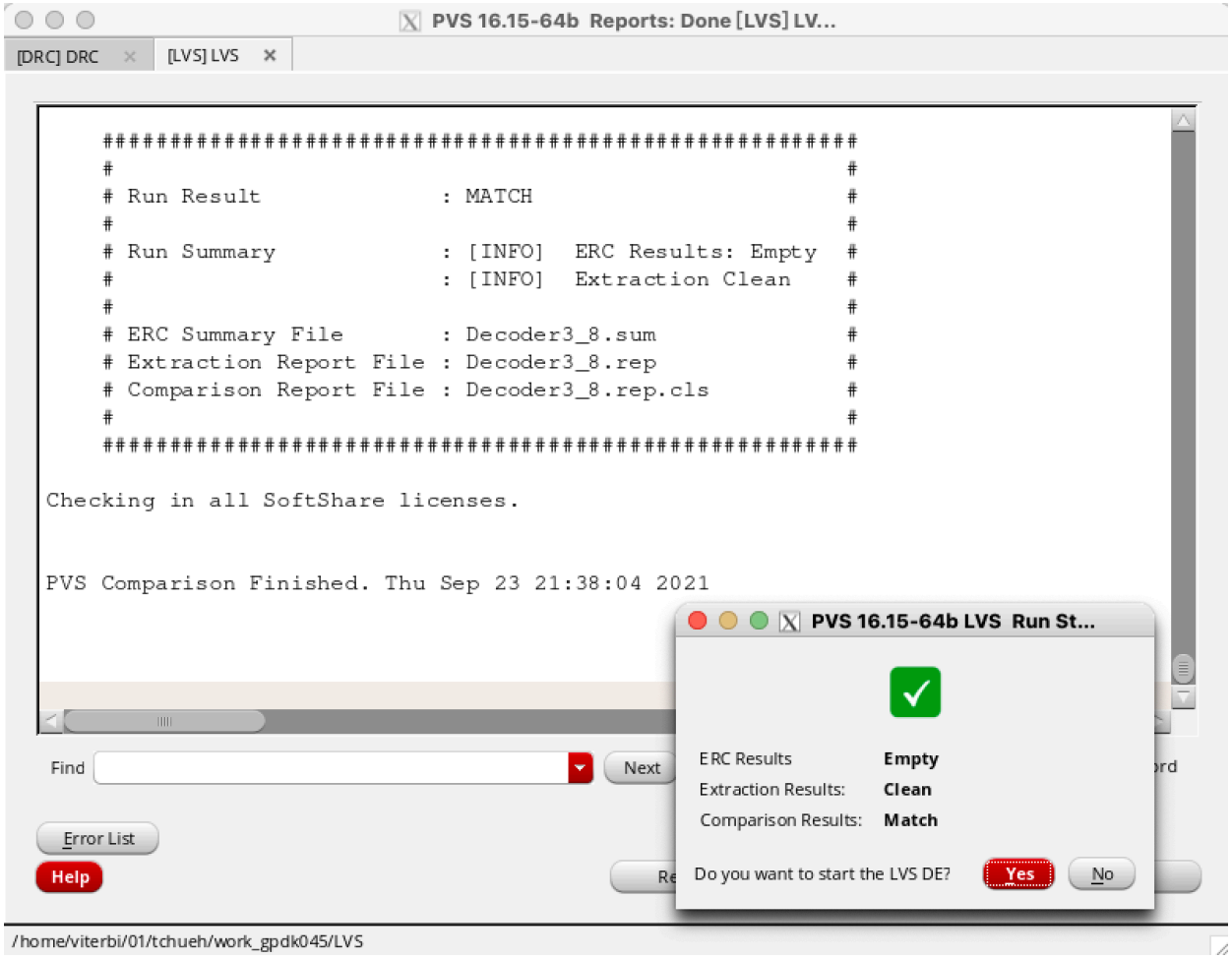
The figure below is the pre-decode system for 3-8 decoder.



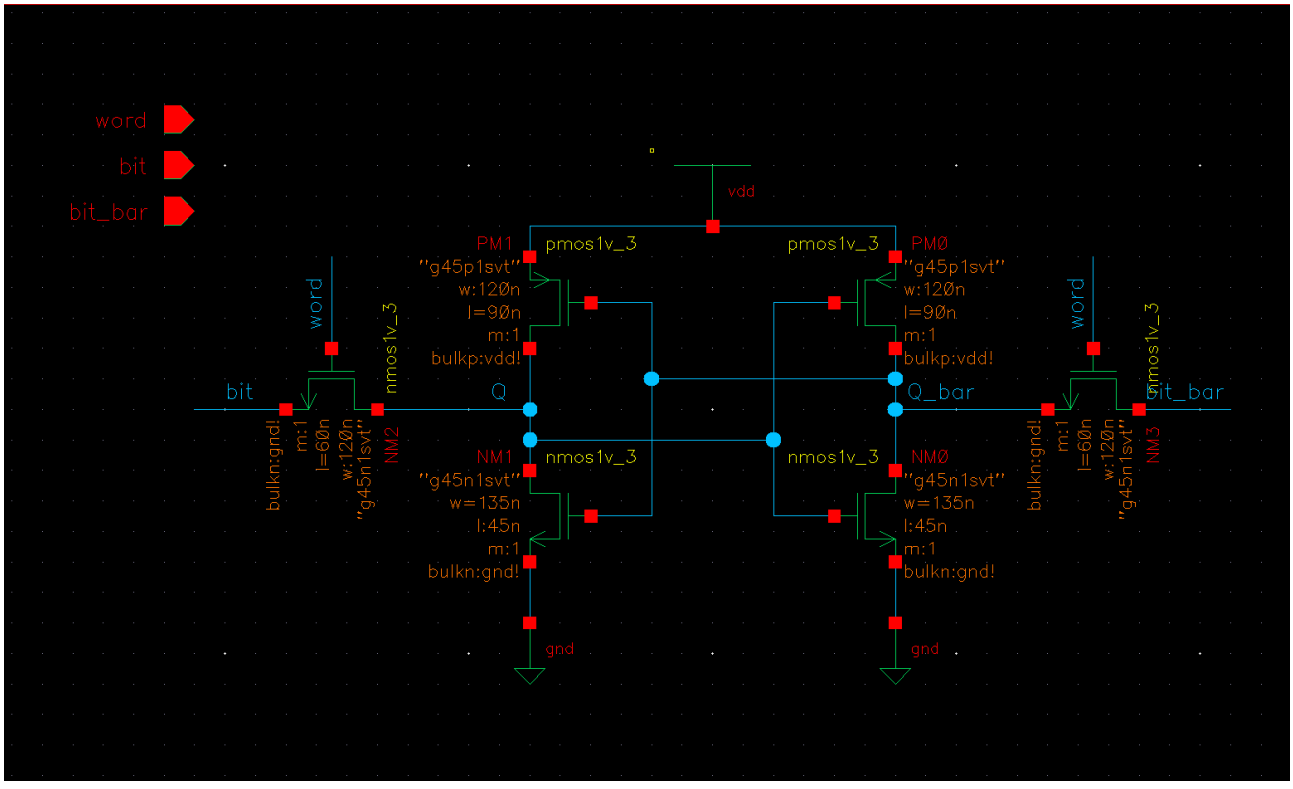
3-8 Decoder (Layout)



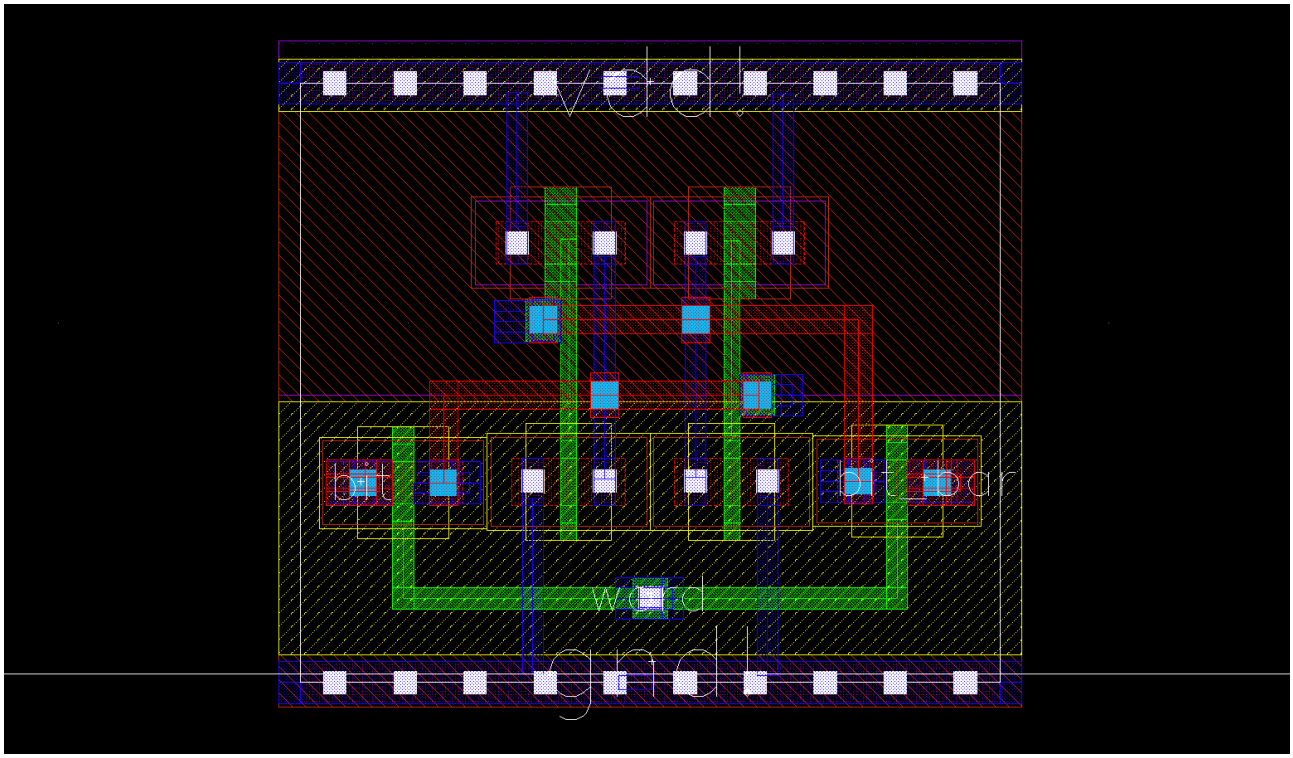


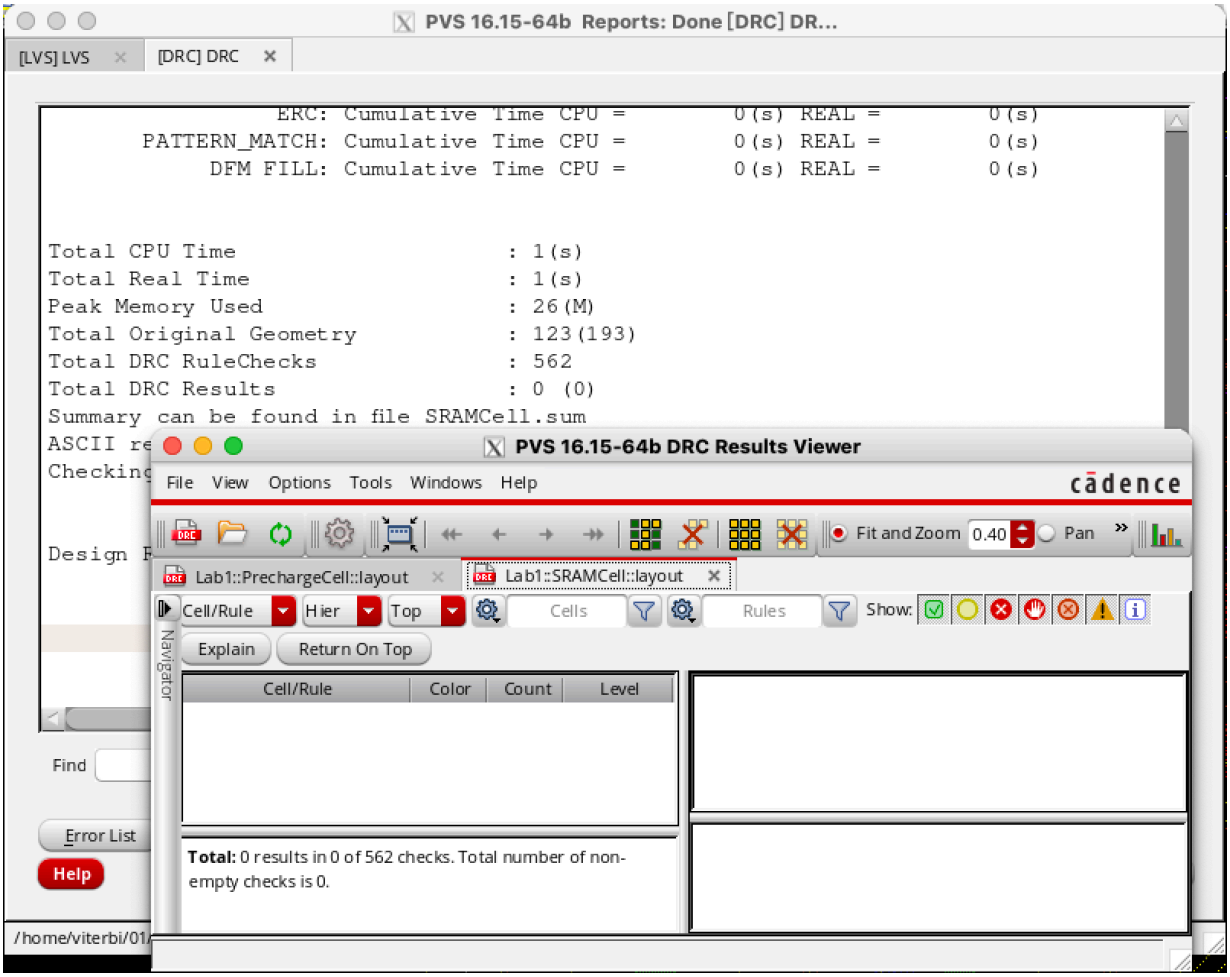


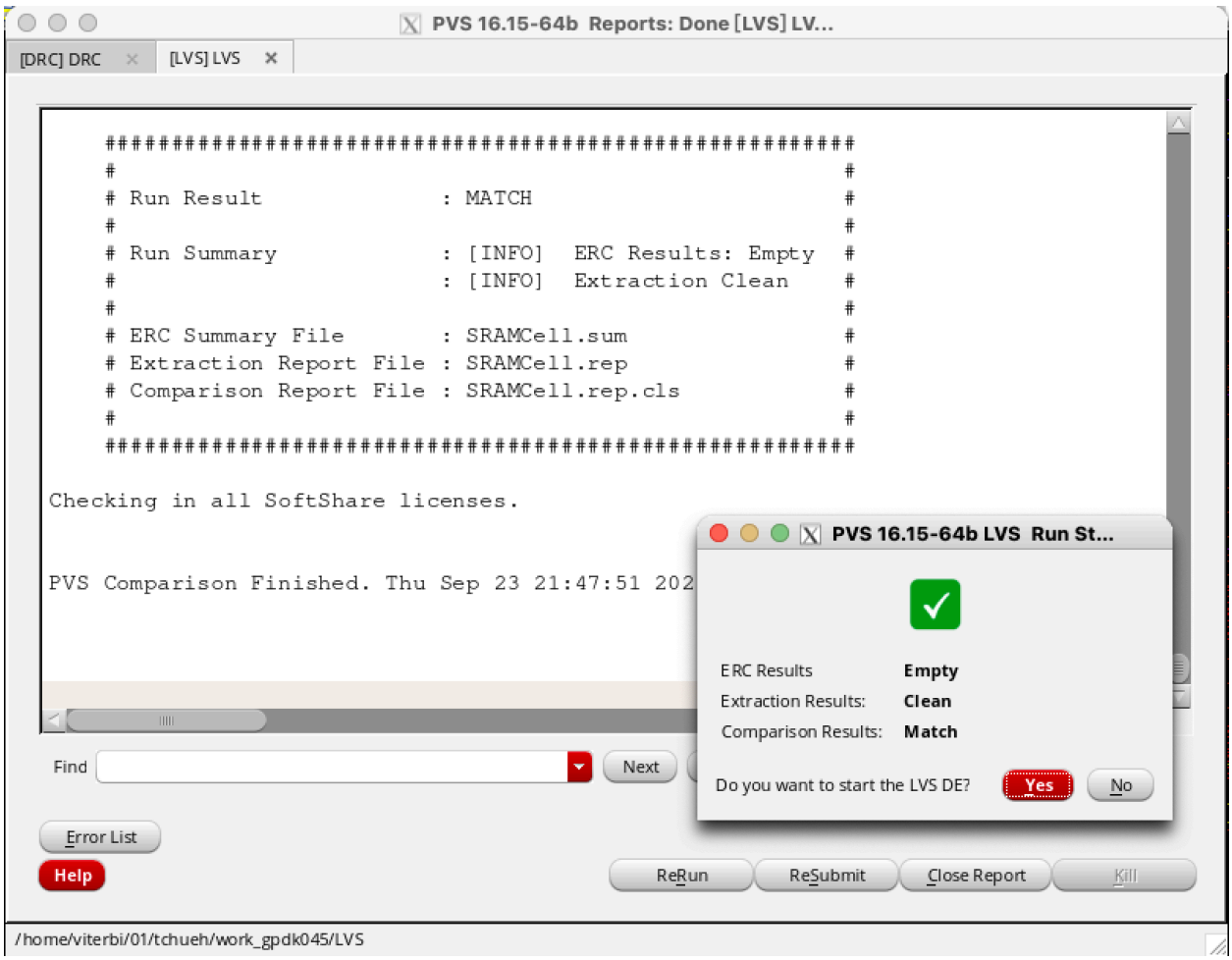
SRAM Cell (Schematic)



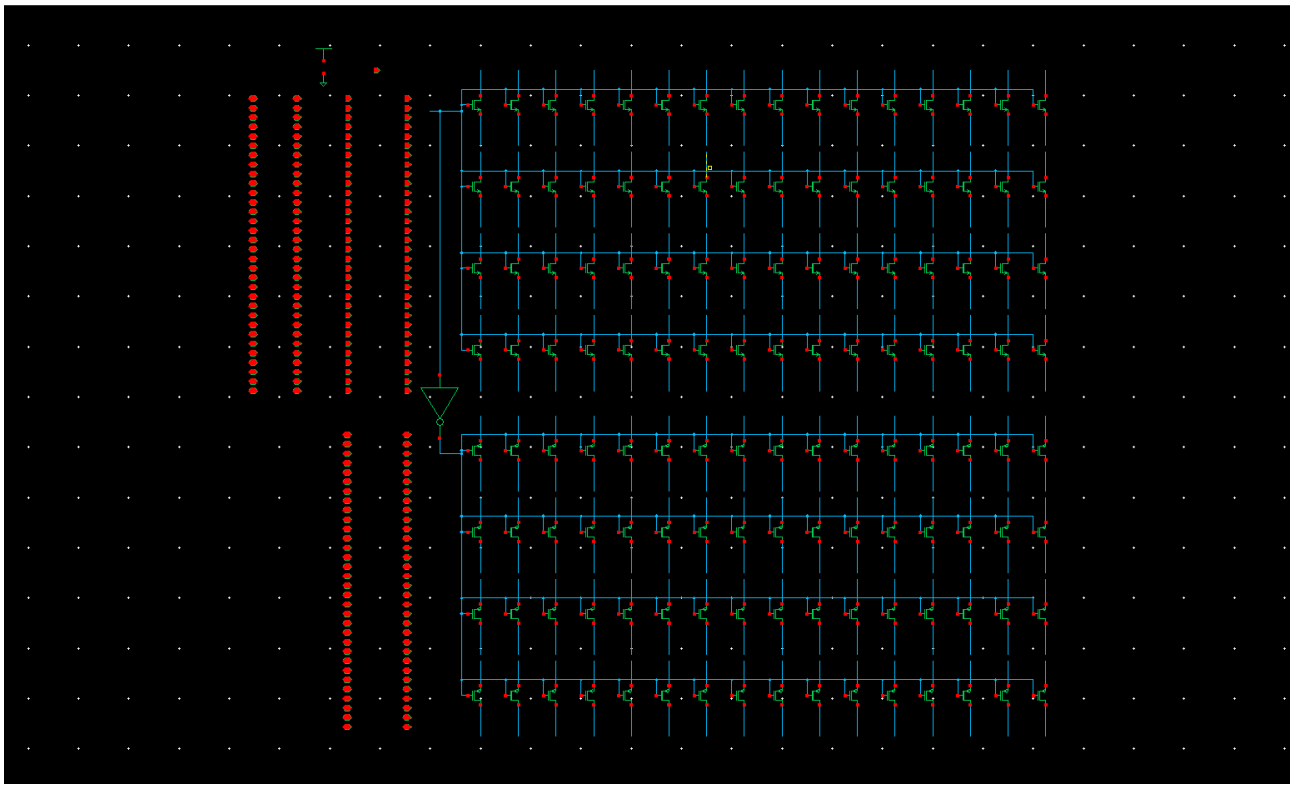
SRAM Cell (Layout)



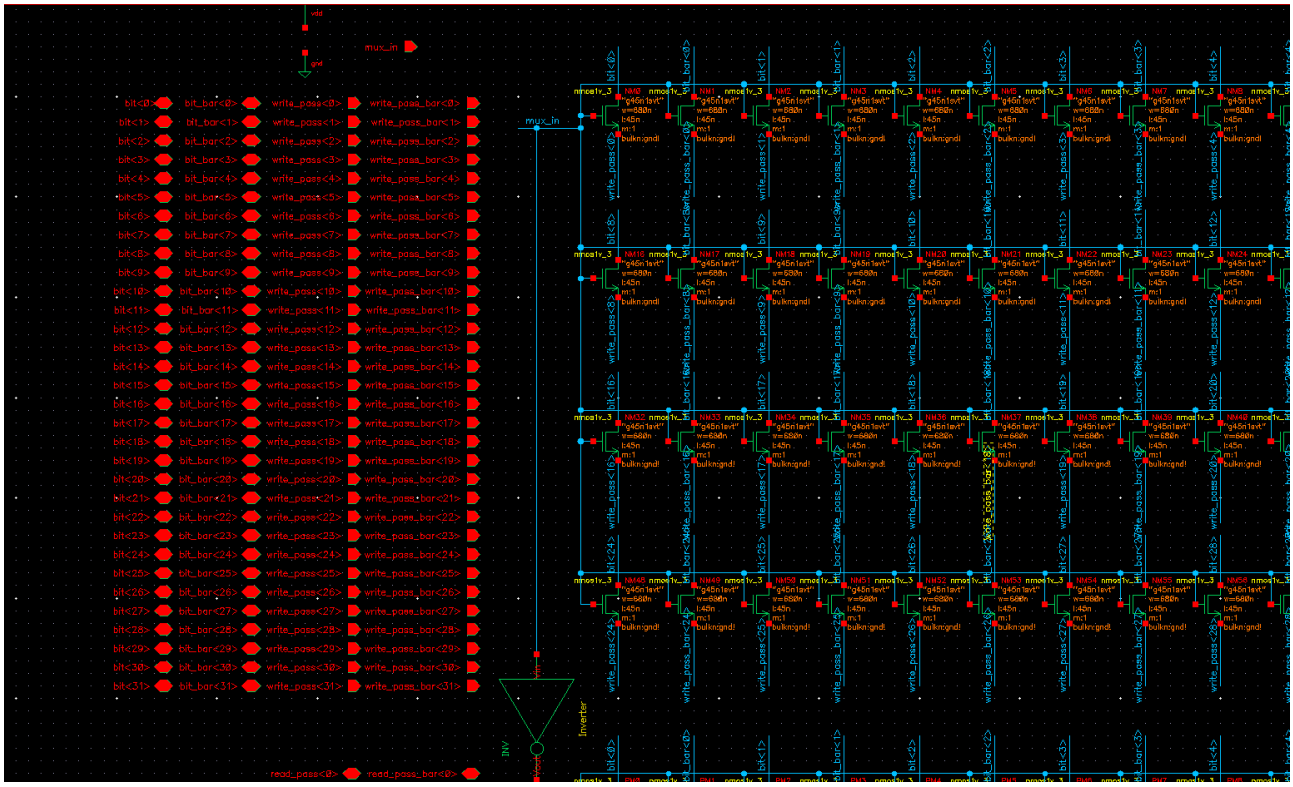




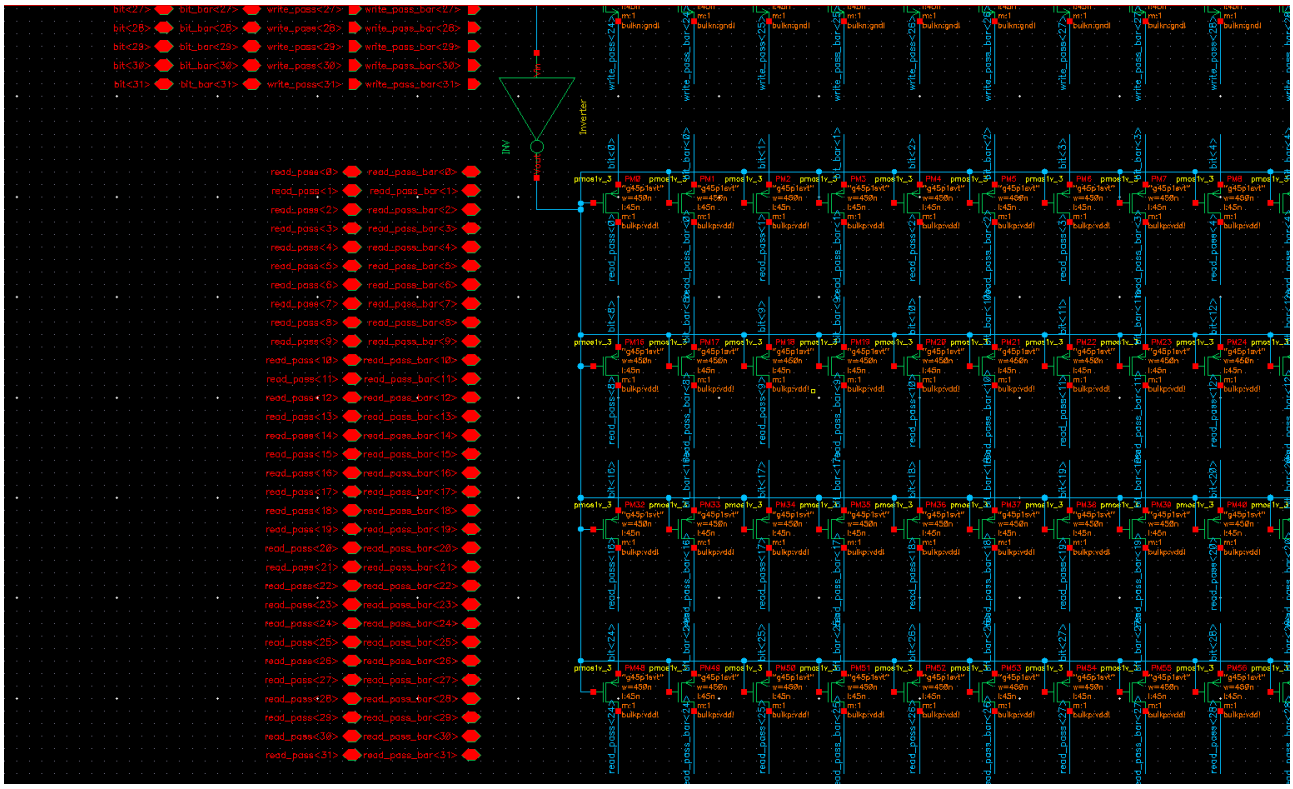
Write/Read MUX (Schematic)



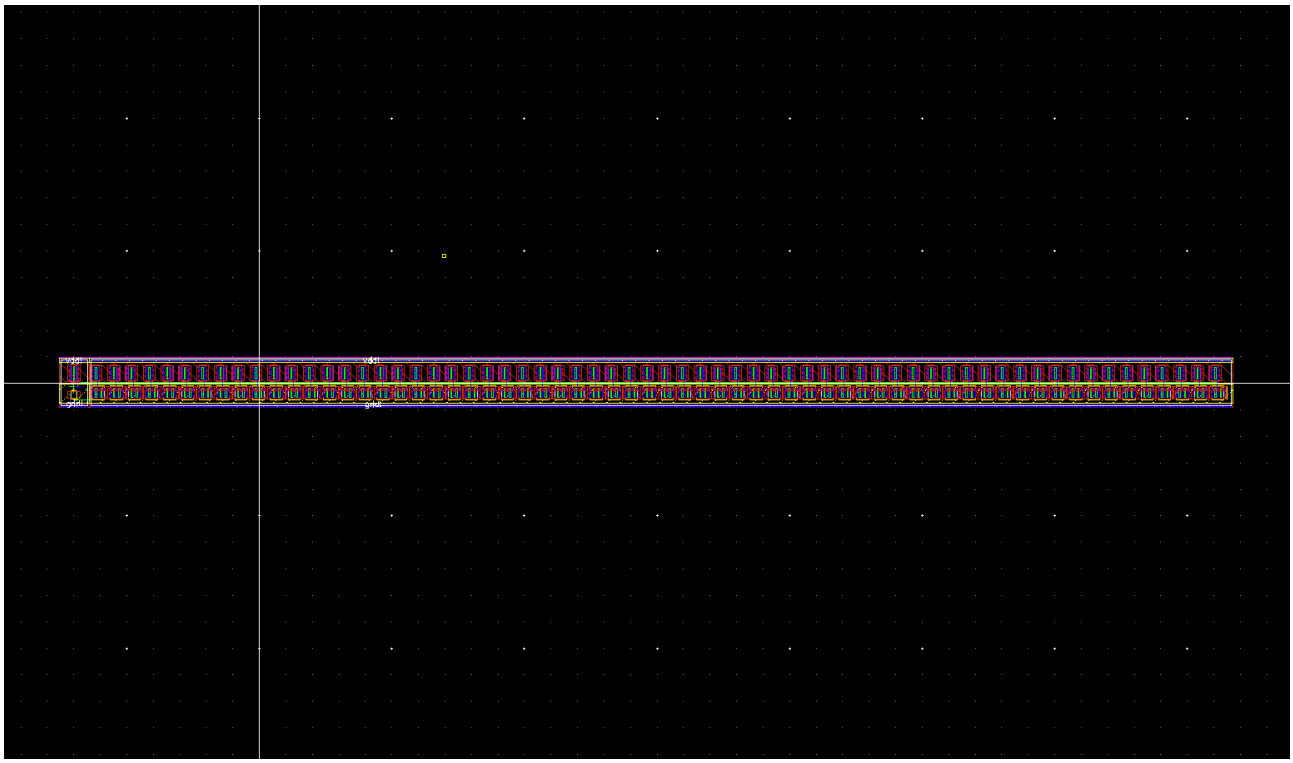
The figure below shows that nMOS pass transistors (W = 680nm / L = 45nm) is used to design the column write MUX.

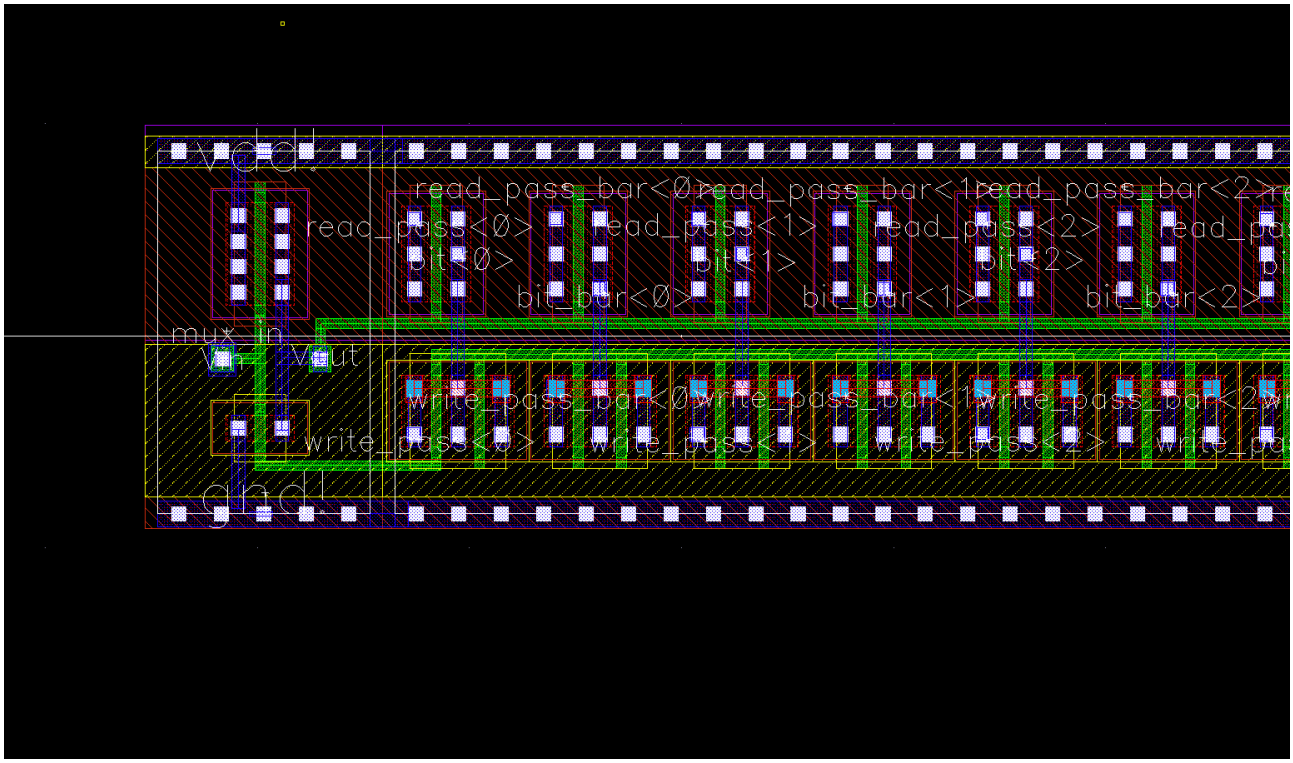


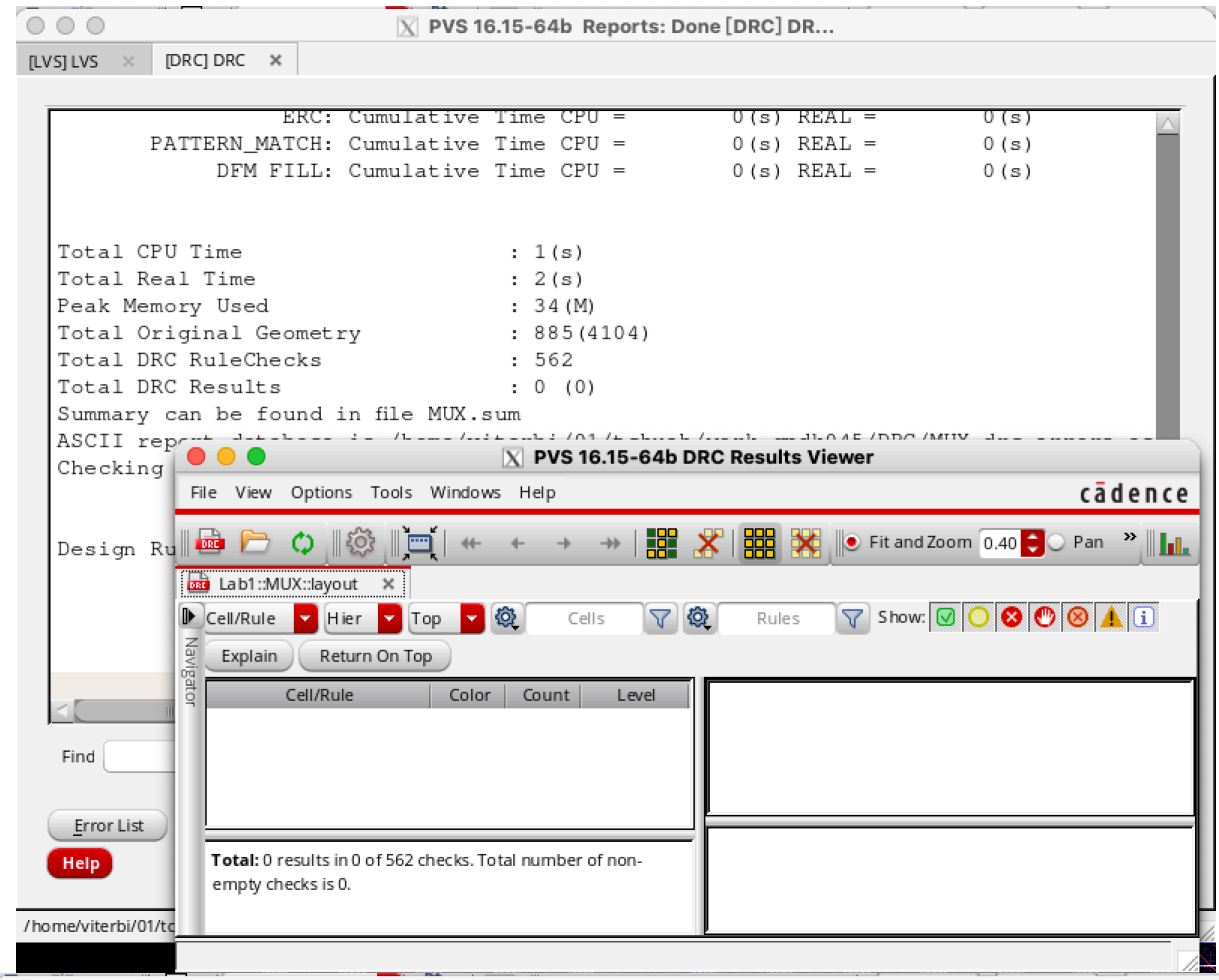
The figure below shows that pMOS pass transistors (W = 450nm / L = 45nm) is used to design the column read MUX.

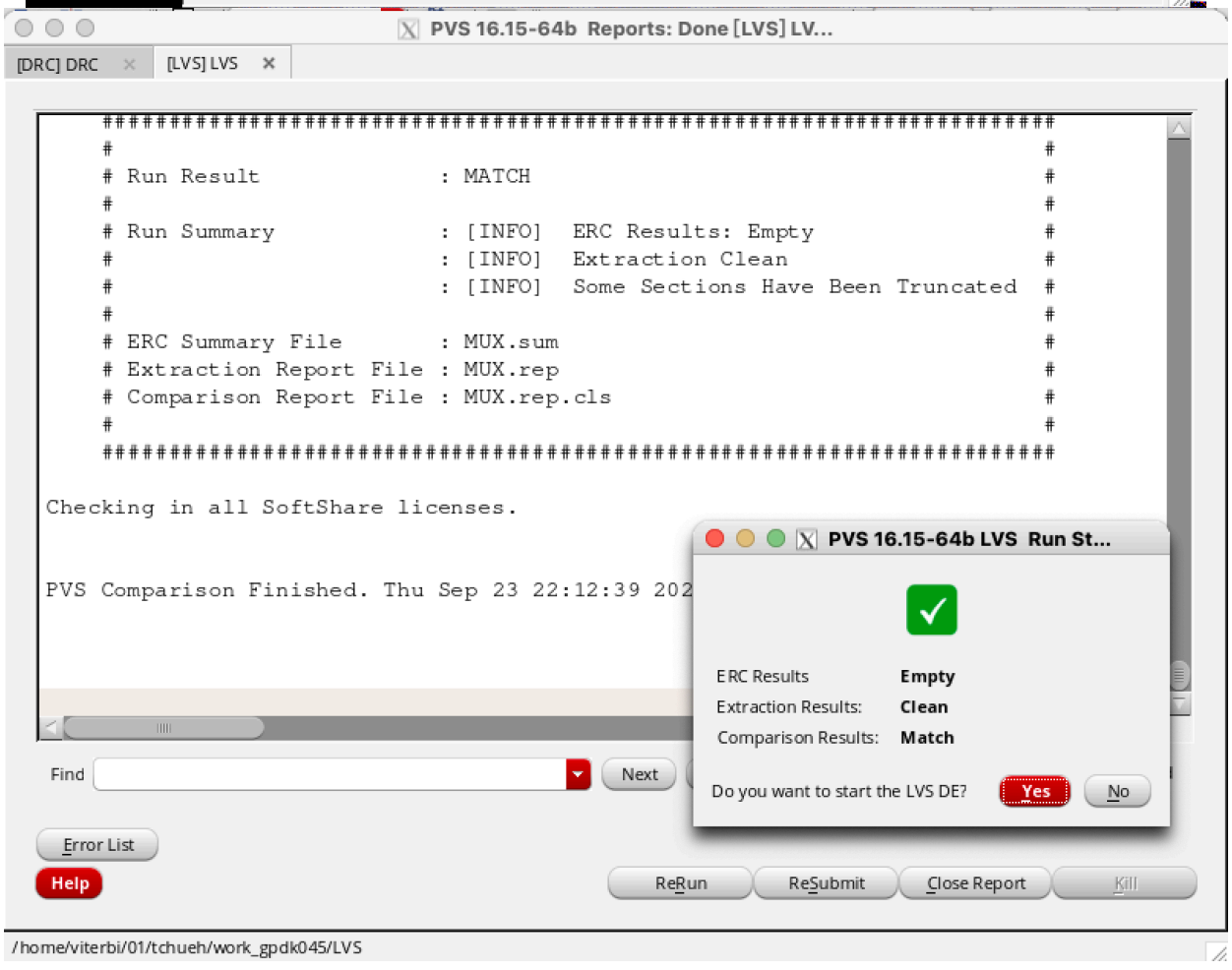


Write/Read MUX (Layout)

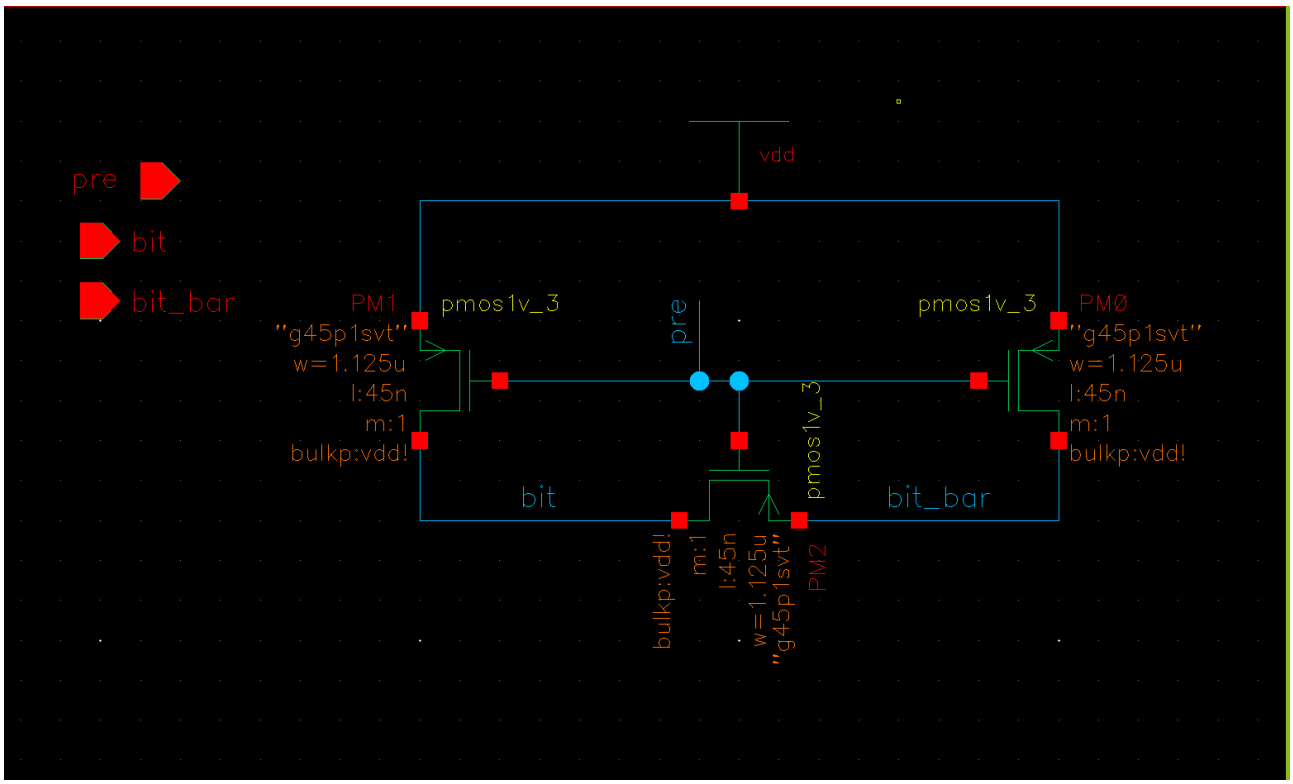




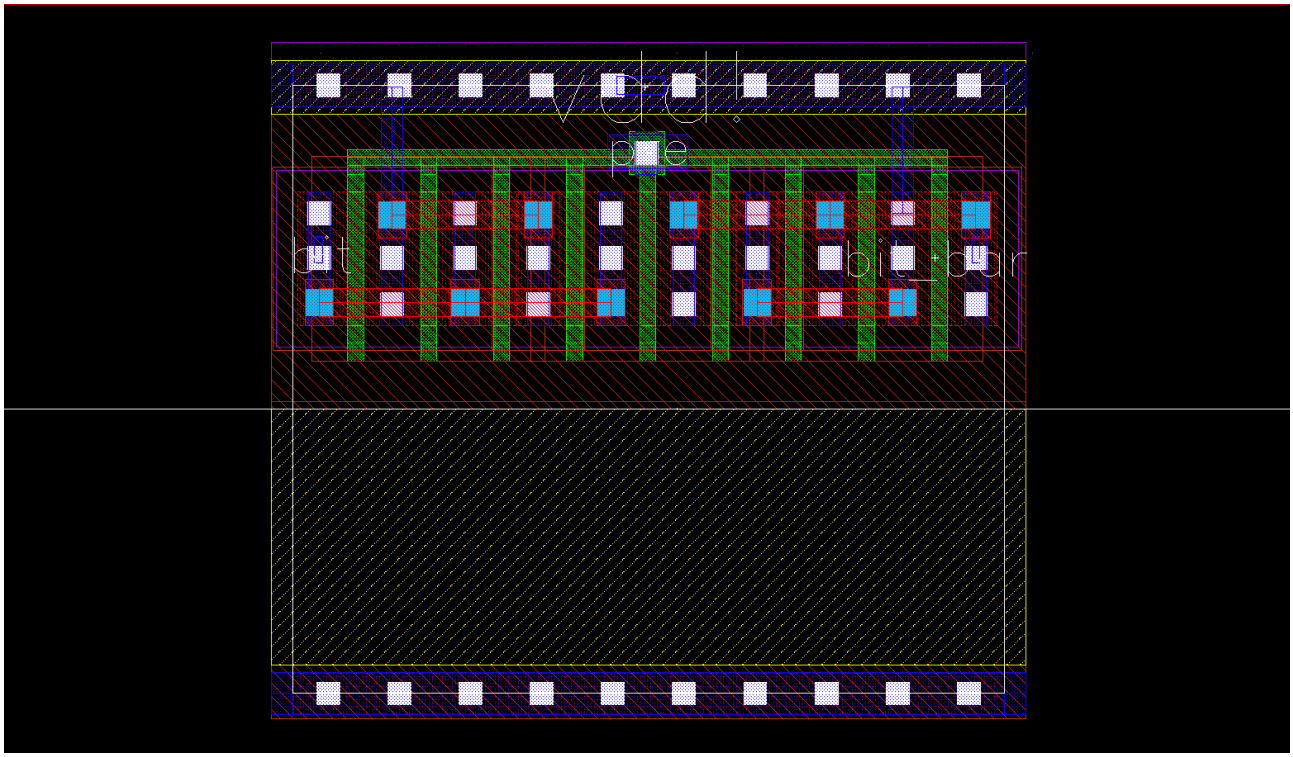

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 2(s)
Peak Memory Used : 34(M)
Total Original Geometry : 885(4104)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file MUX.sum
Checking
Design Ru
Find
Error List
Help
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::MUX::layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.
/home/viterbi/01/tc

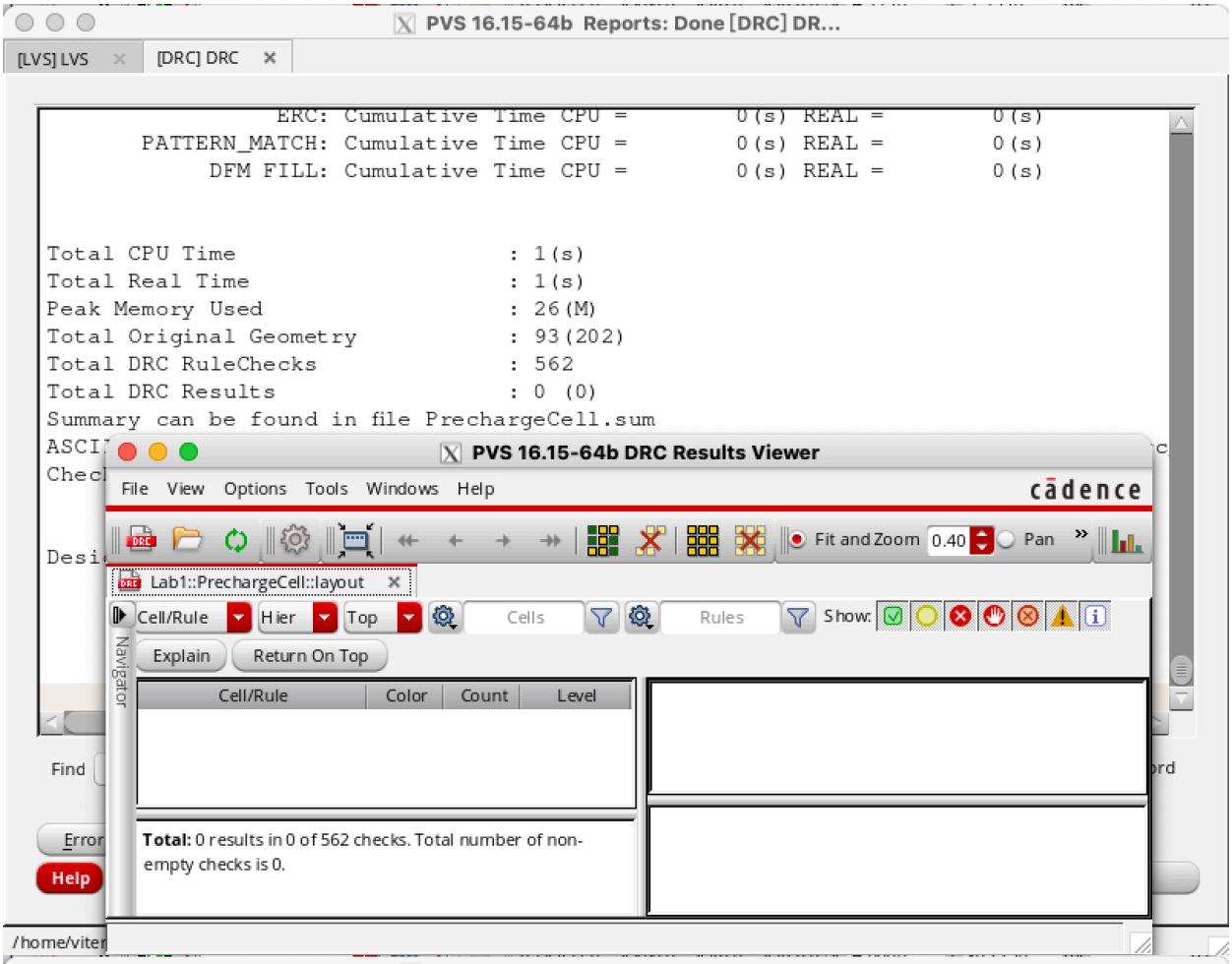

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
: [INFO] Some Sections Have Been Truncated
ERC Summary File : MUX.sum
Extraction Report File : MUX.rep
Comparison Report File : MUX.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 22:12:39 202
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

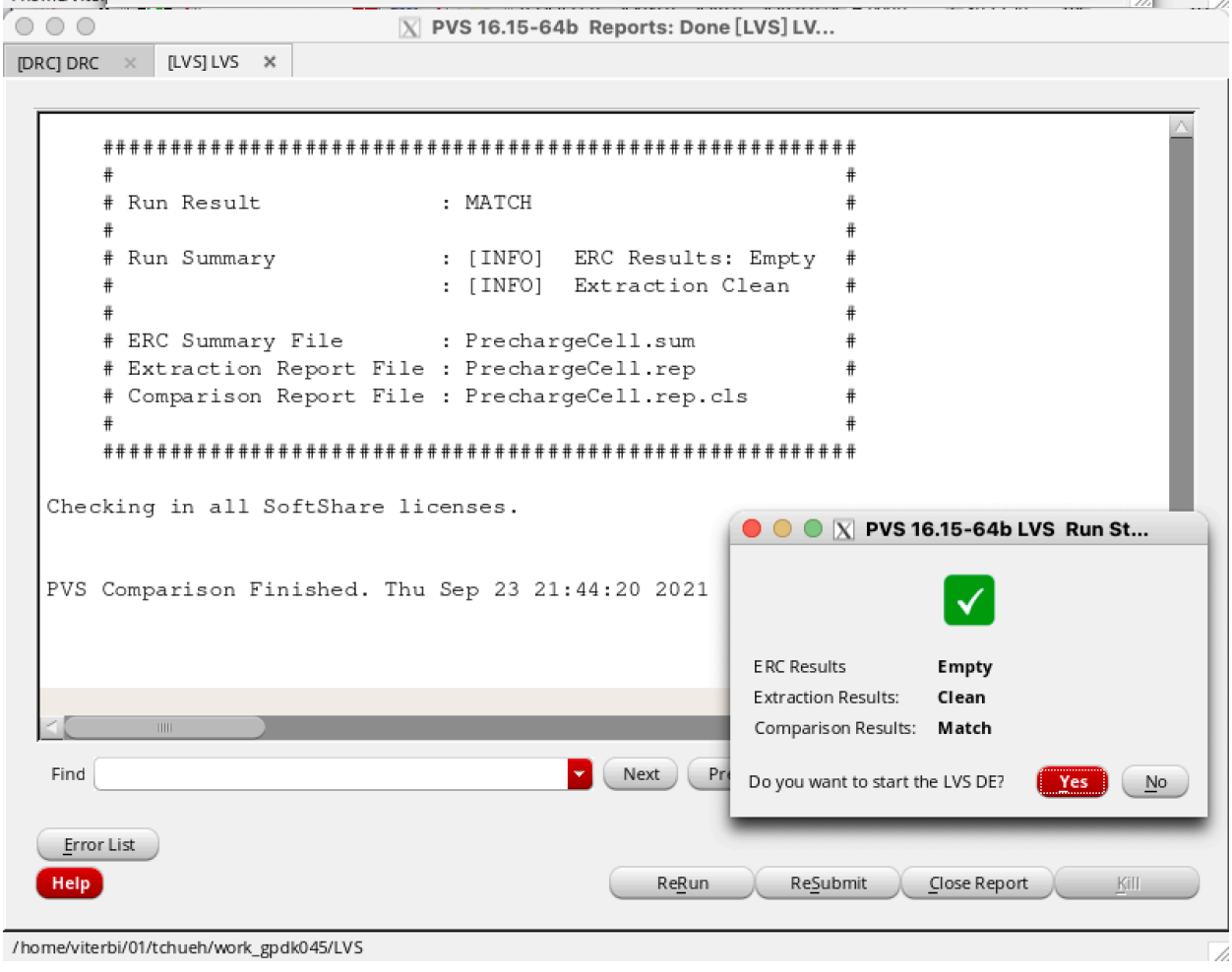
Pre-charge (Schematic)



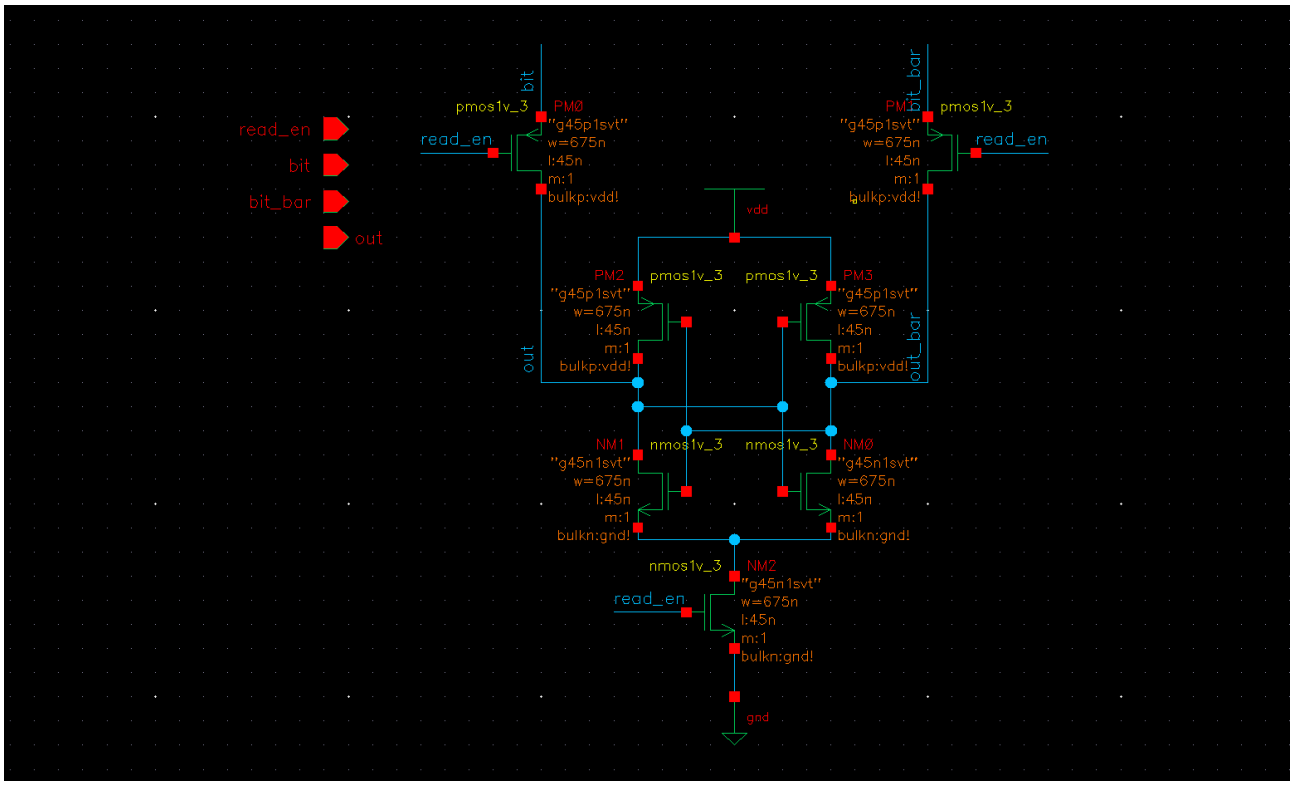
Pre-charge (Layout)



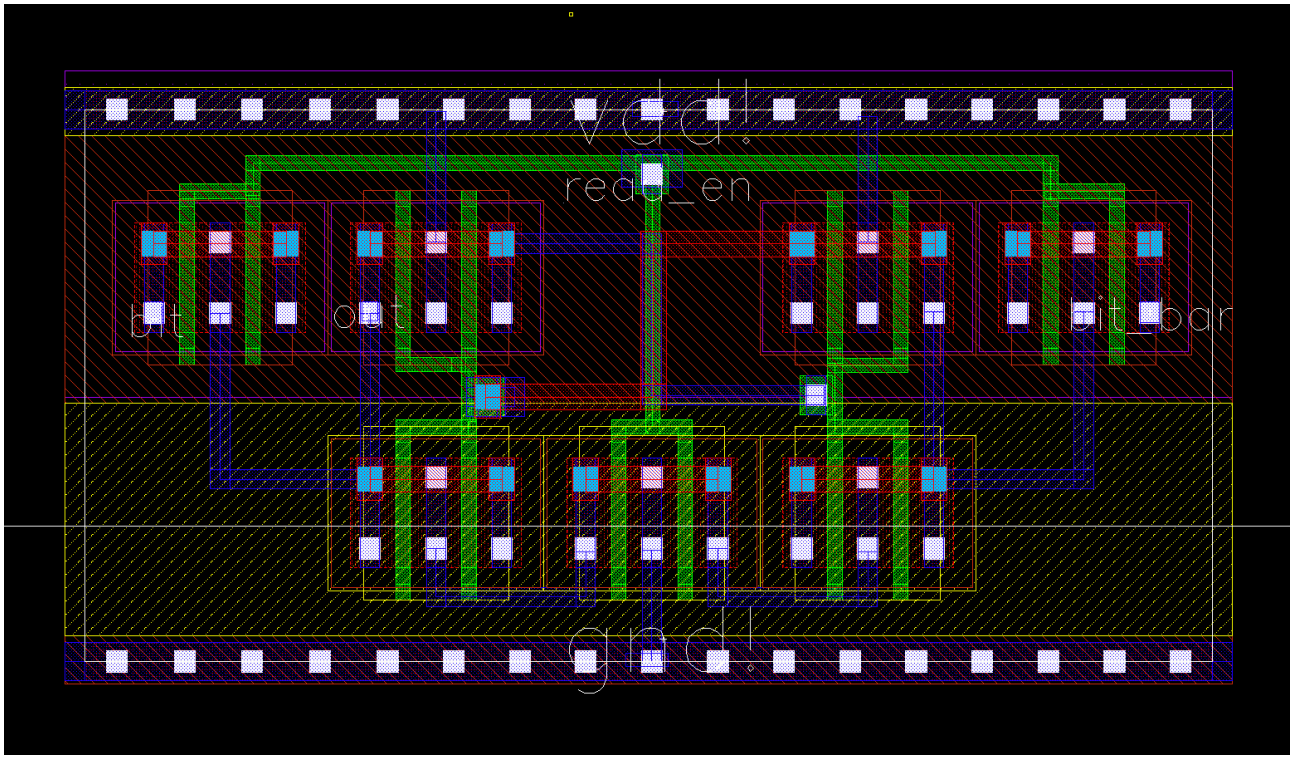

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used : 26(M)
Total Original Geometry : 93(202)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file PrechargeCell.sum
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::PrechargeCell::layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.
Find
Error
Help

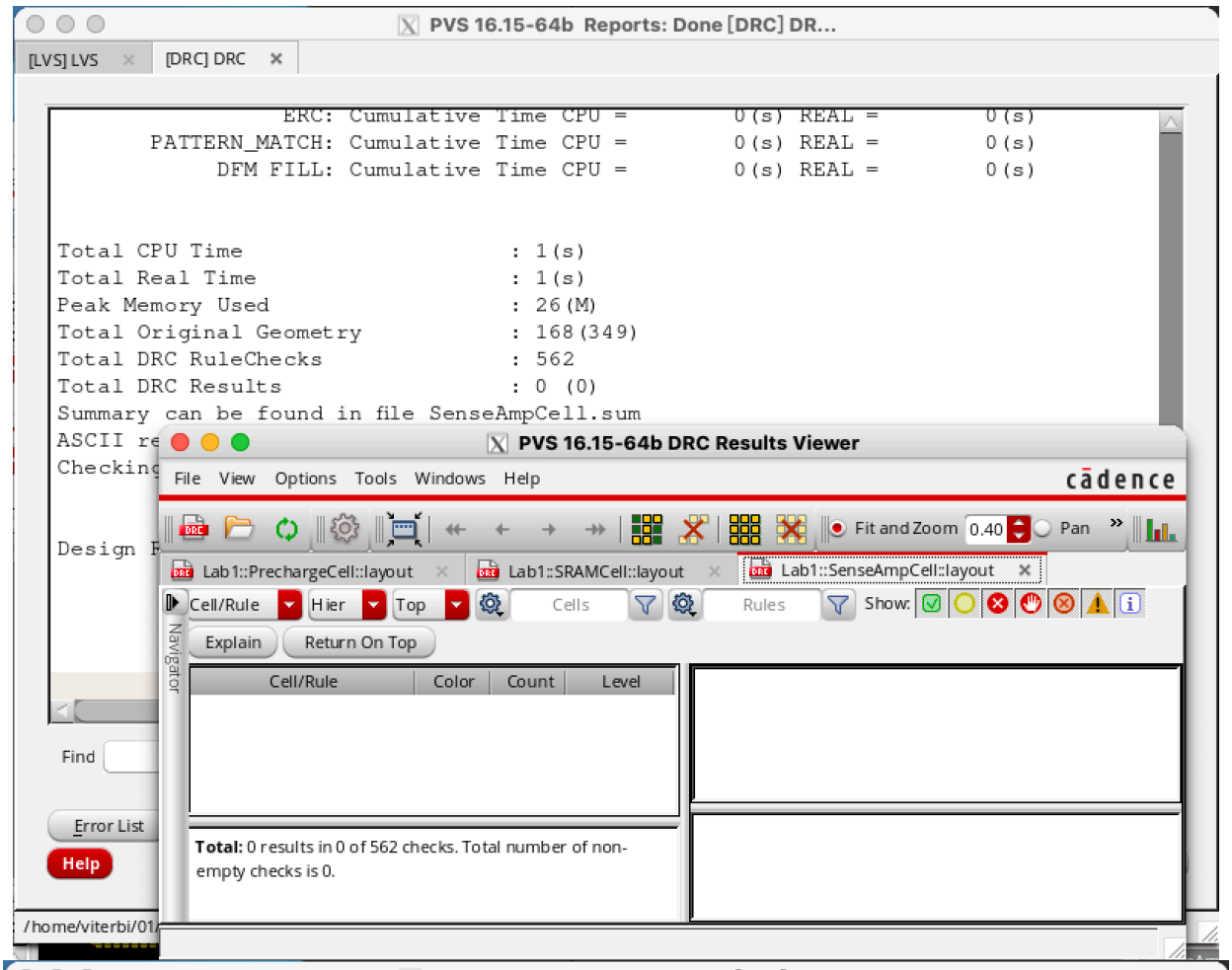

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : PrechargeCell.sum
Extraction Report File : PrechargeCell.rep
Comparison Report File : PrechargeCell.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 21:44:20 2021
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE? Yes No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

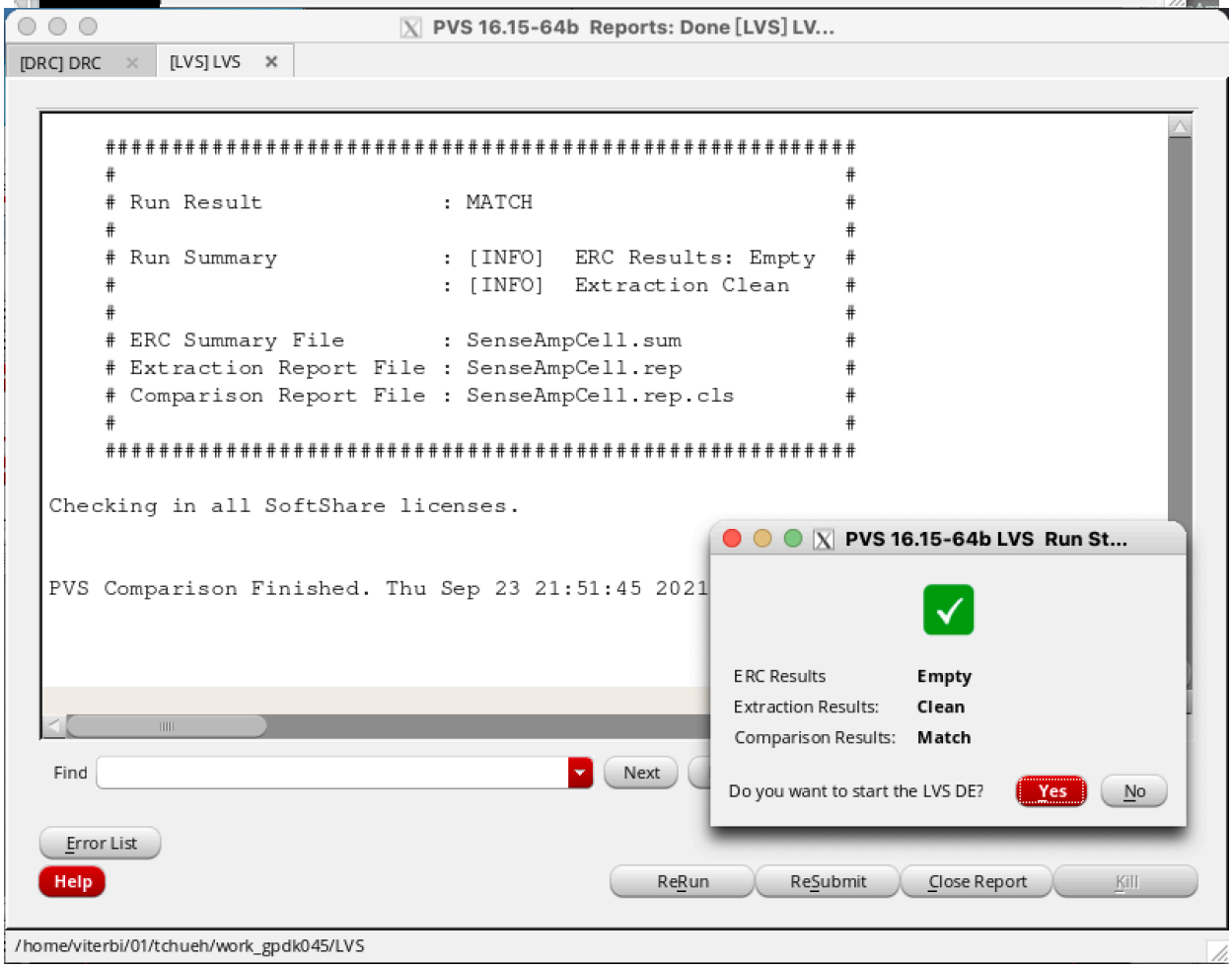
Sense Amp. (Schematic)



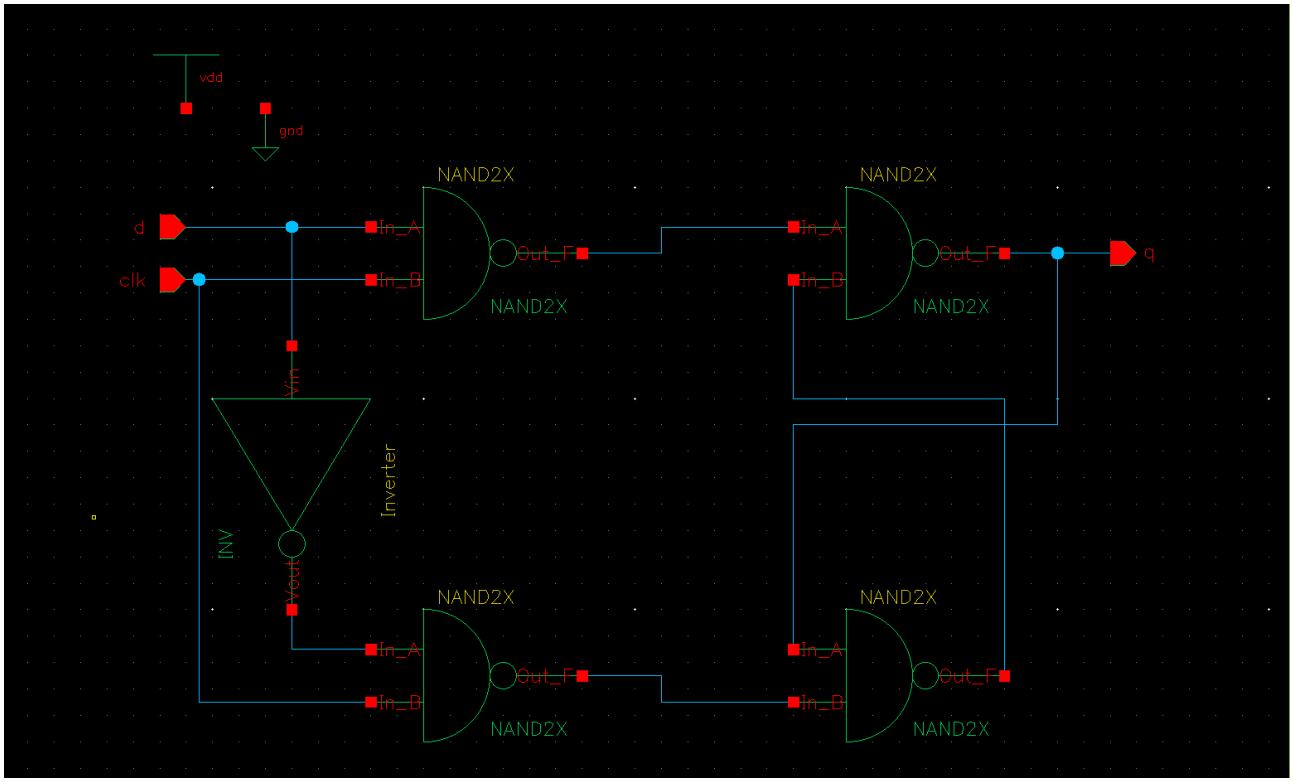
Sense Amp. (Layout)



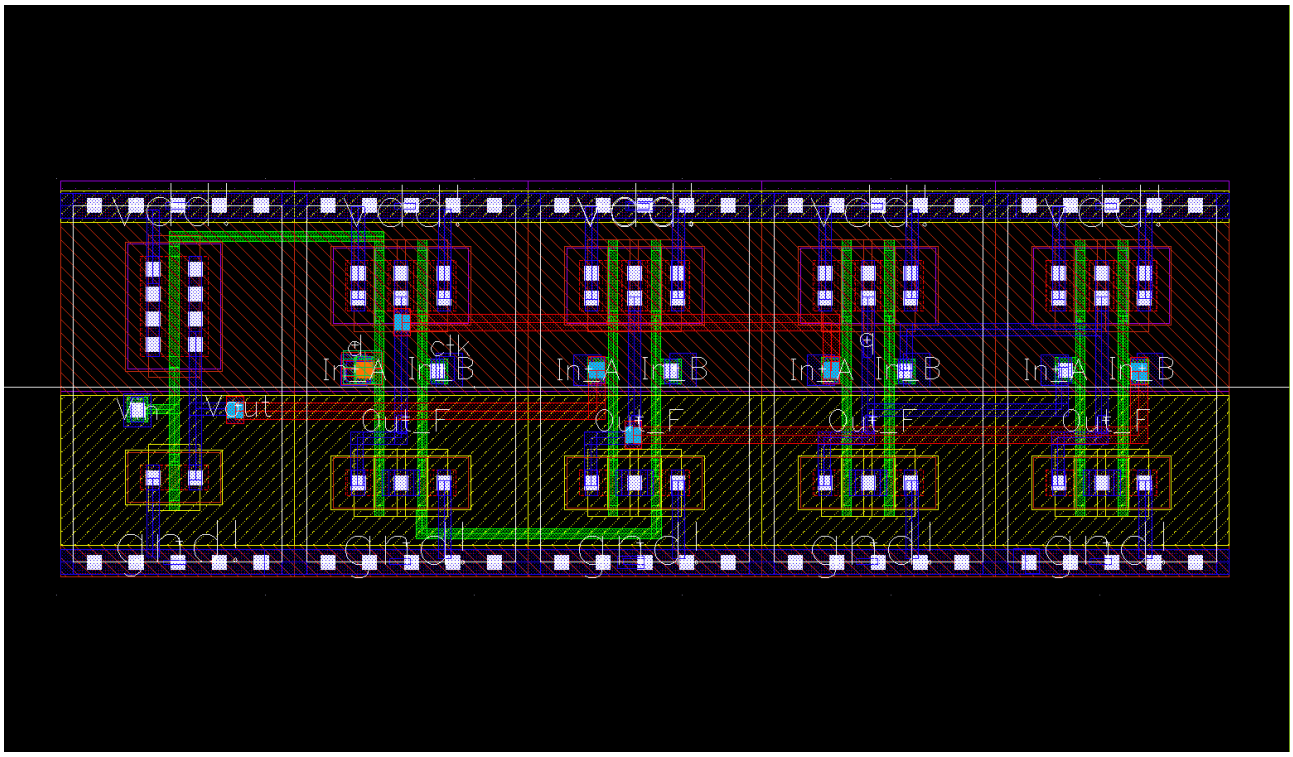

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0 (s) REAL = 0 (s)
PATTERN_MATCH: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DFM FILL: Cumulative Time CPU = 0 (s) REAL = 0 (s)
Total CPU Time : 1 (s)
Total Real Time : 1 (s)
Peak Memory Used : 26 (M)
Total Original Geometry : 168 (349)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file SenseAmpCell.sum
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::PrechargeCell::layout
Lab1::SRAMCell::layout
Lab1::SenseAmpCell::layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.
Find
Error List
Help
/home/viterbi/01

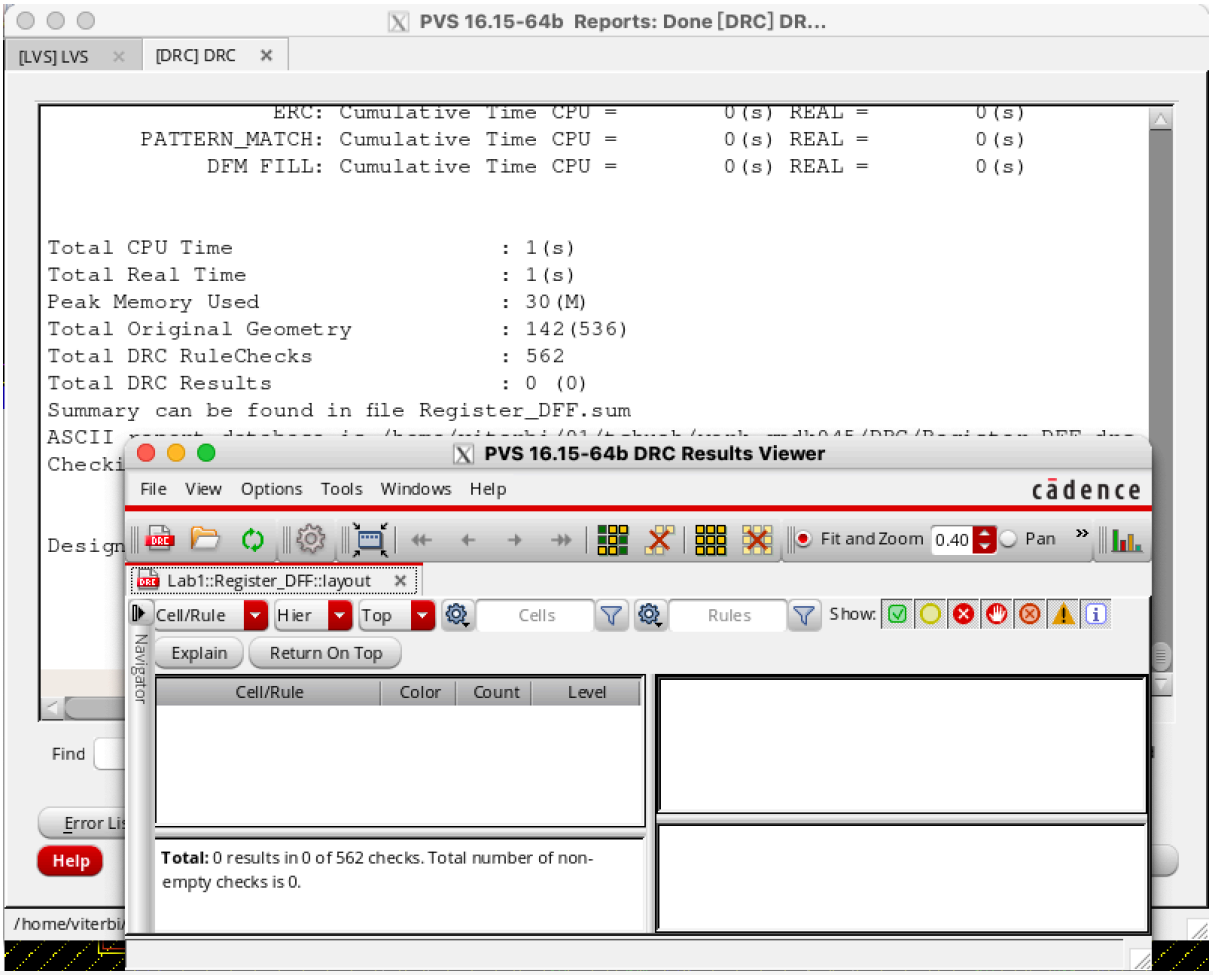

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : SenseAmpCell.sum
Extraction Report File : SenseAmpCell.rep
Comparison Report File : SenseAmpCell.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 21:51:45 2021
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

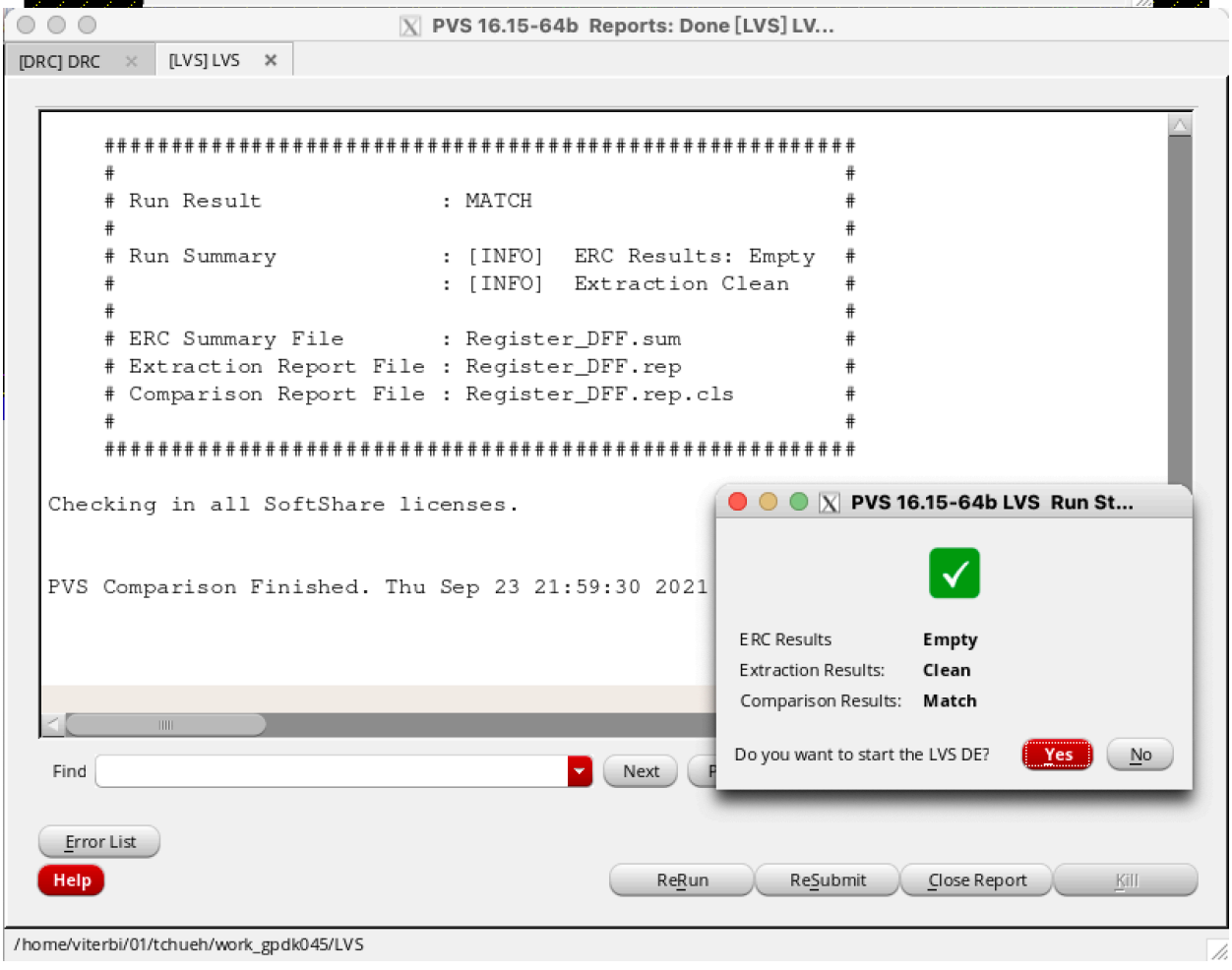
Register (Schematic)



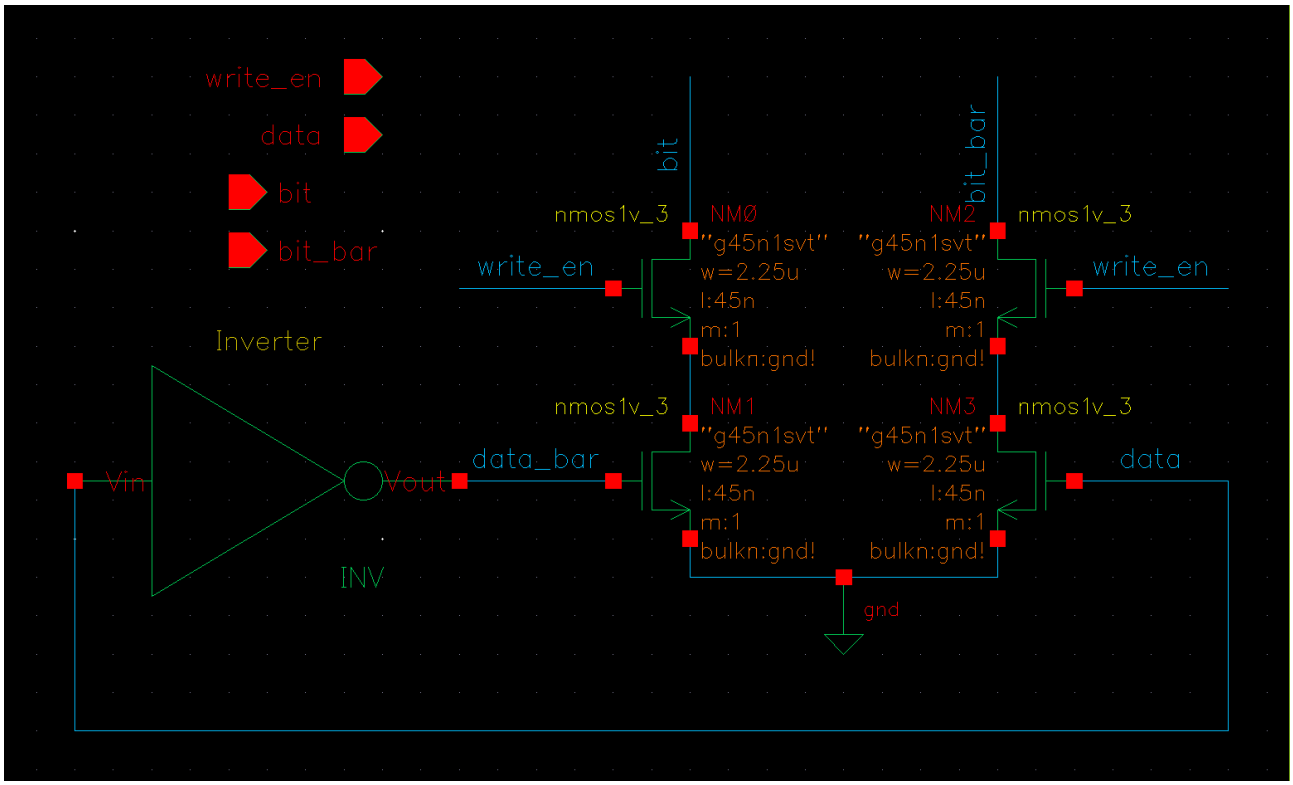
Register (Layout)



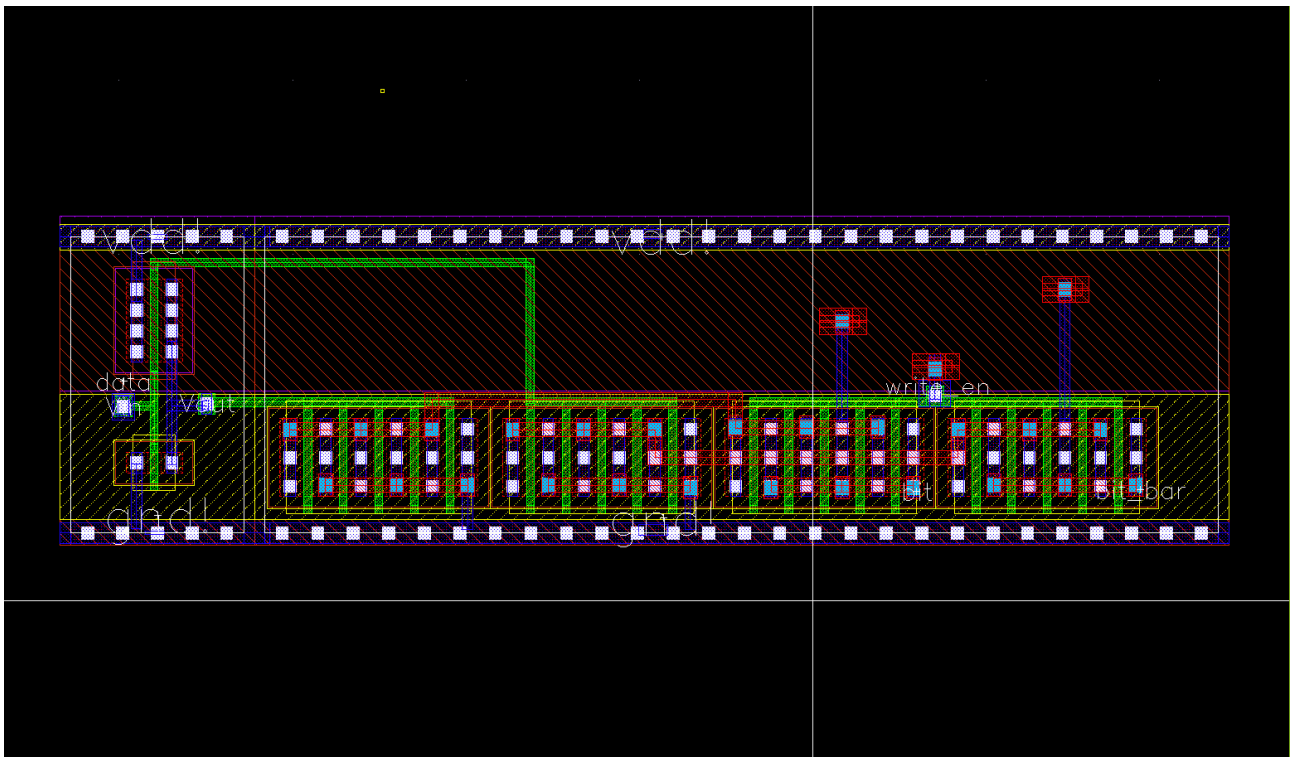

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used : 30(M)
Total Original Geometry : 142(536)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Register_DFF.sum
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::Register_DFF::layout
Cell/Rule Hier Top Cells Rules Show:
Explain Return On Top
Navigator
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.
Find
Error Li
Help
/home/viterbi

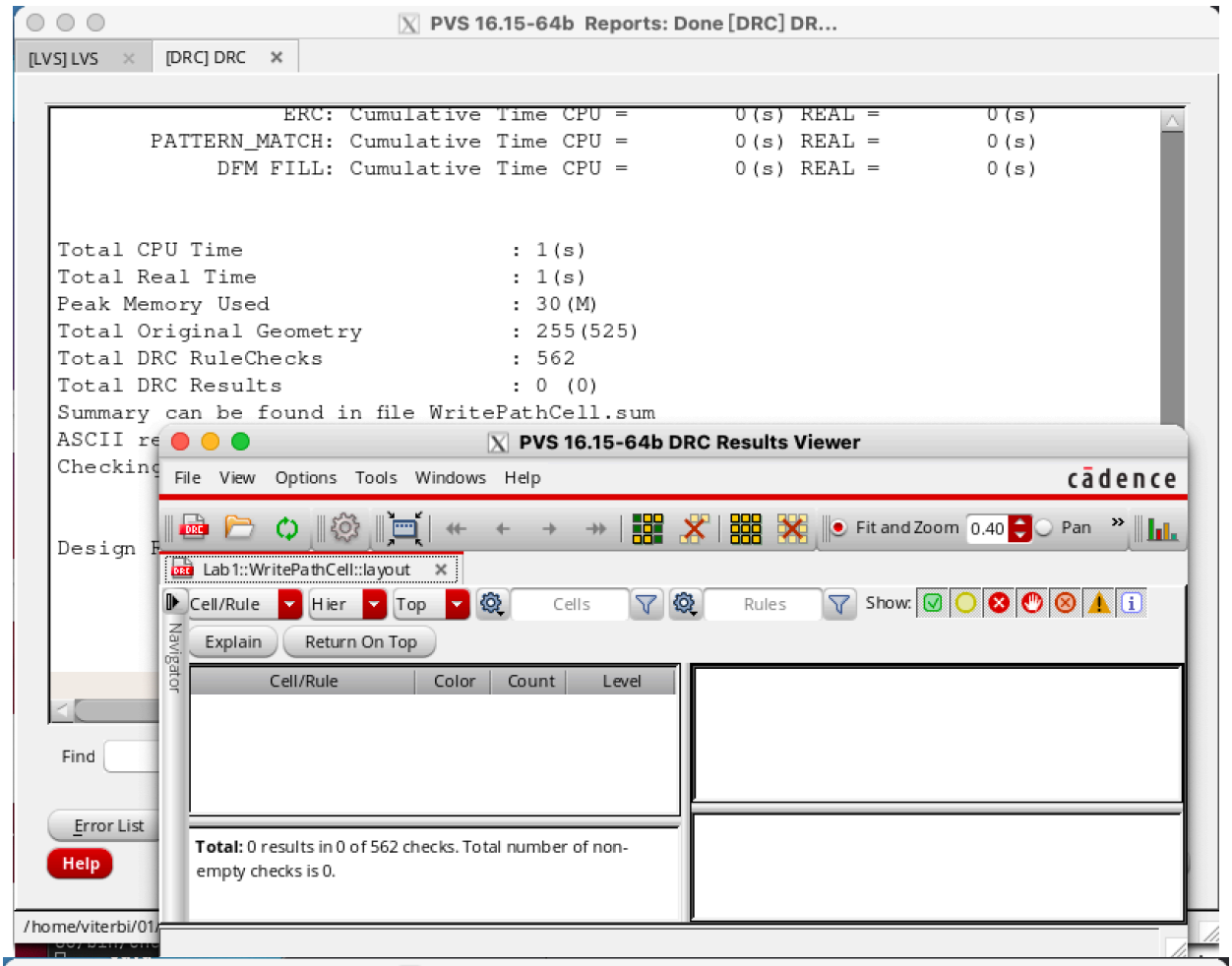

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : Register_DFF.sum
Extraction Report File : Register_DFF.rep
Comparison Report File : Register_DFF.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 21:59:30 2021
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

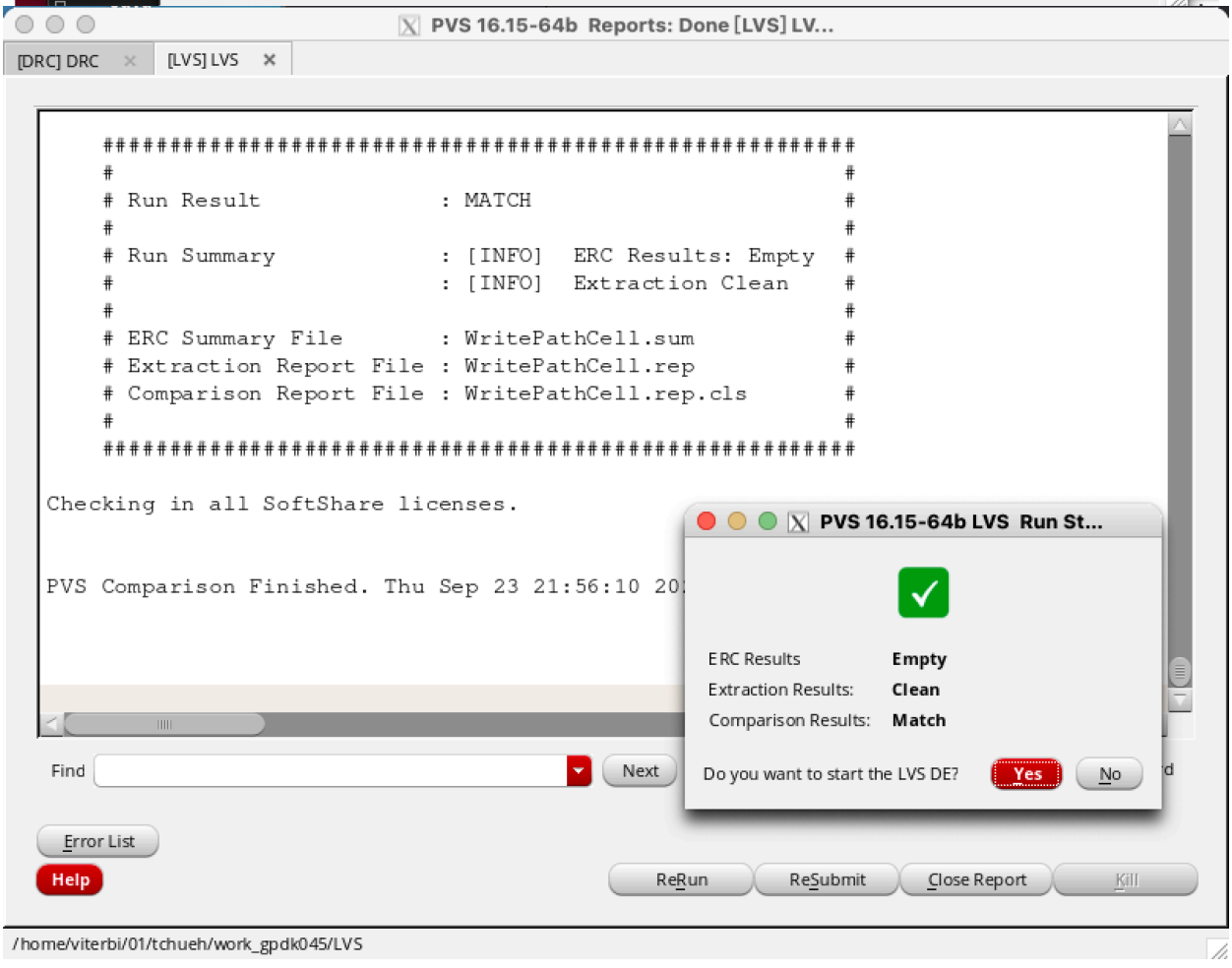
Write Path (Schematic)



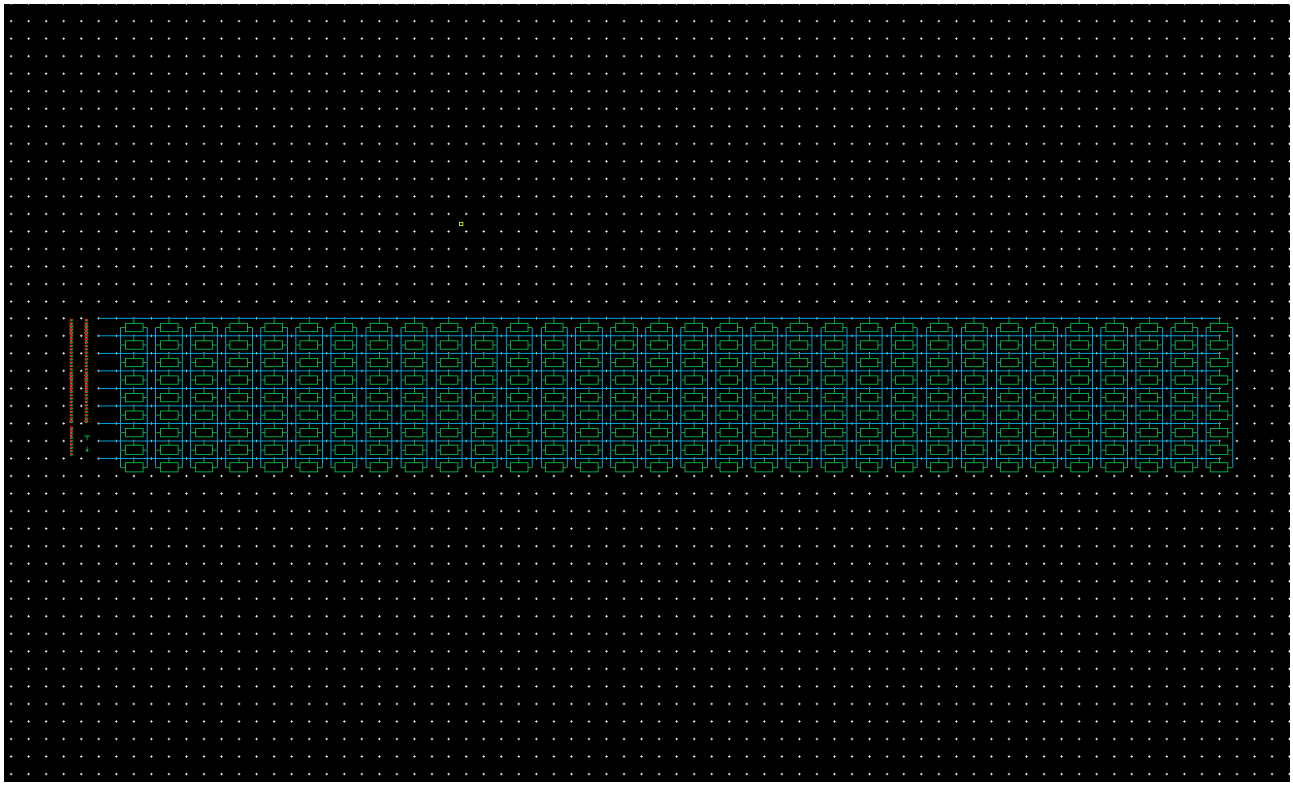
Write Path (Layout)



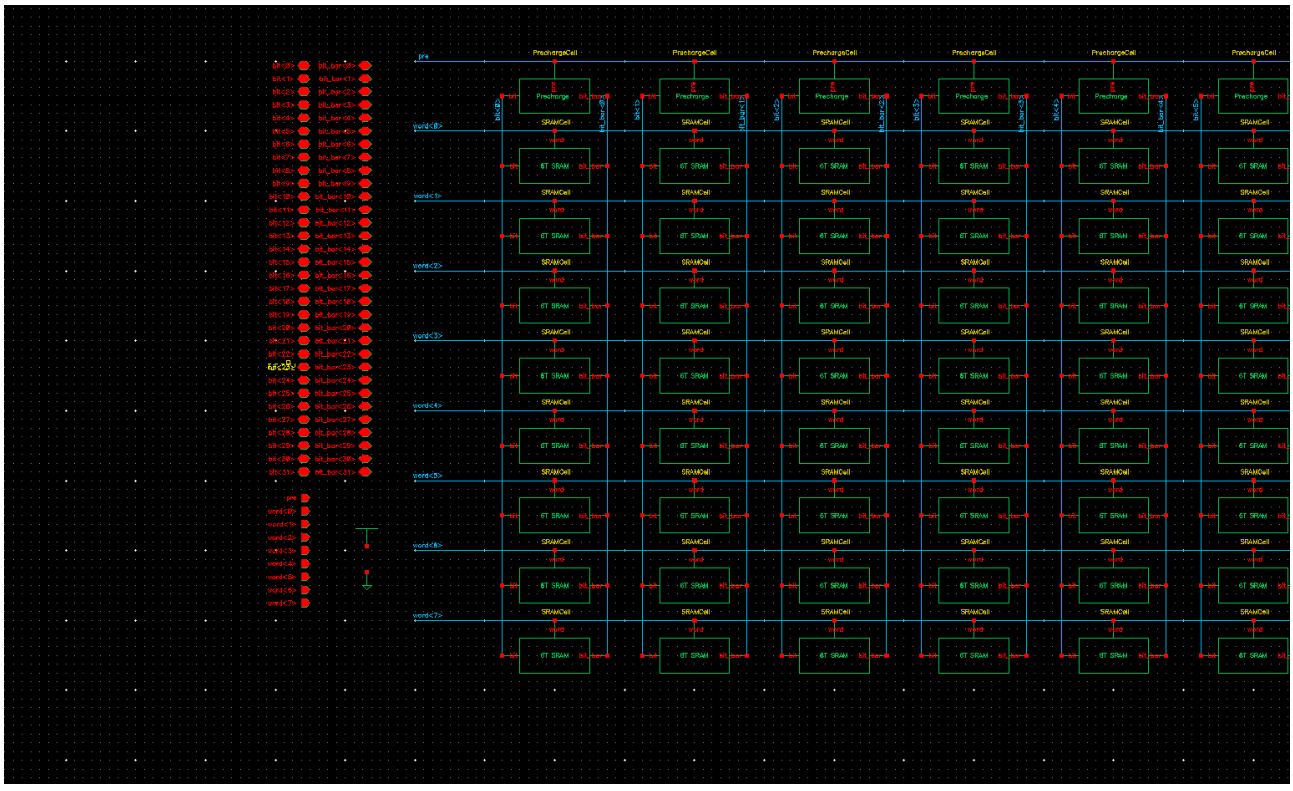

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used : 30(M)
Total Original Geometry : 255(525)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file WritePathCell.sum
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::WritePathCell::layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.
Find
Error List
Help
/home/viterbi/01


PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : WritePathCell.sum
Extraction Report File : WritePathCell.rep
Comparison Report File : WritePathCell.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 21:56:10 20
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

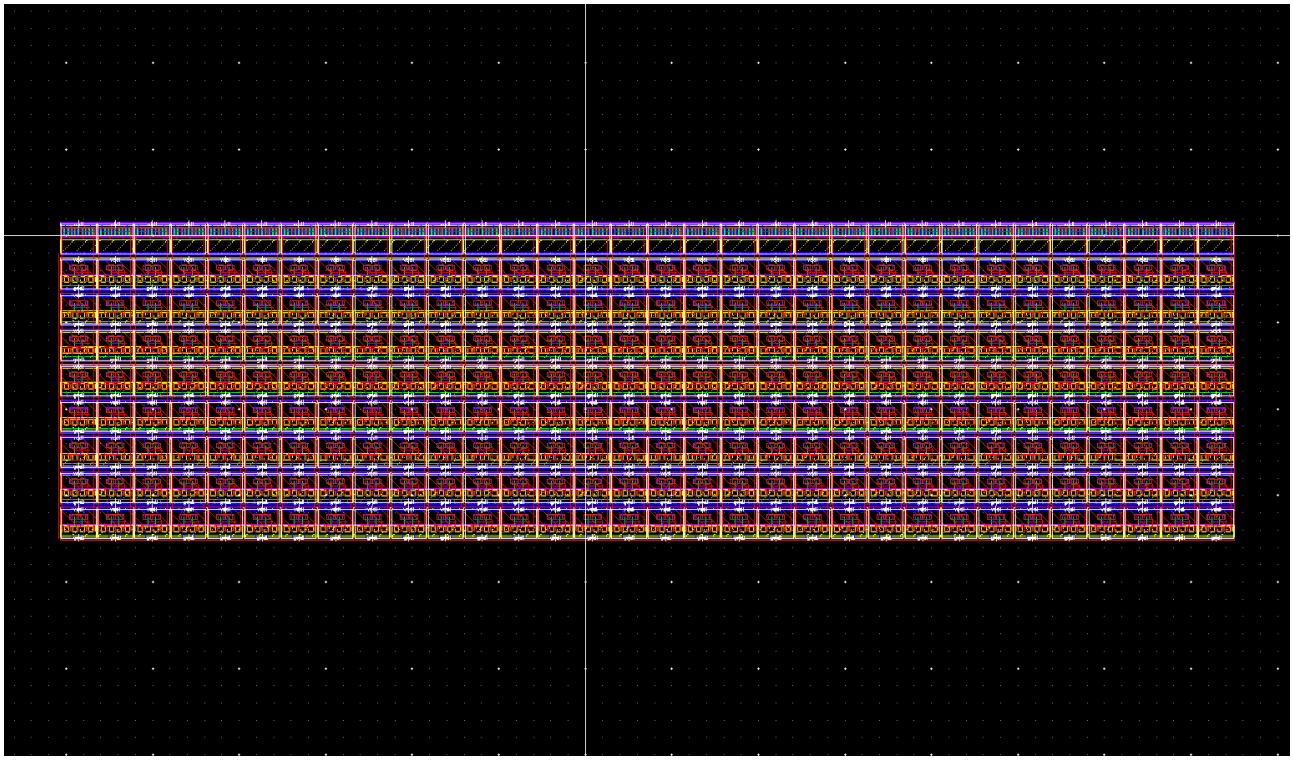
SRAM 8x32 Bank (Schematic)



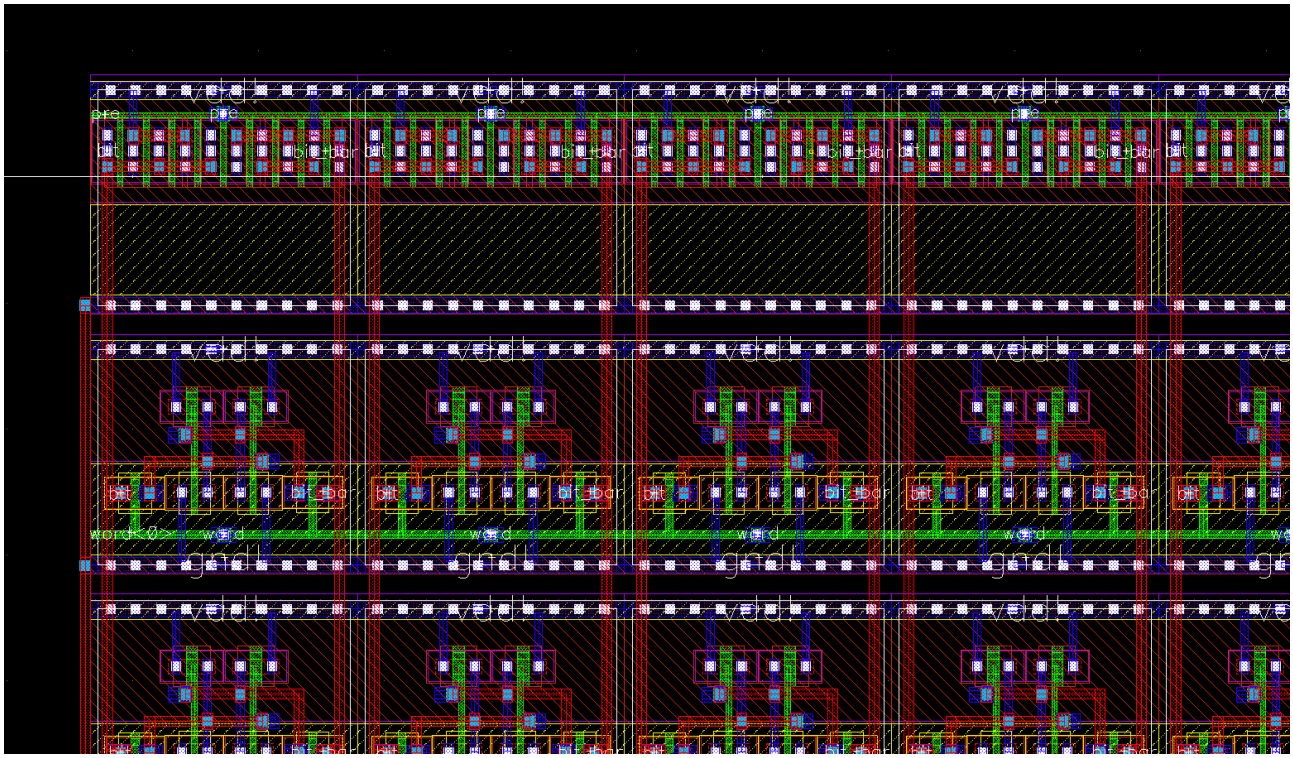
Each 256-bit SRAM bank was constructed with 8 row, 32 columns. The pre-charge was placed at the first row and connected to all the bit line and bit line bars.

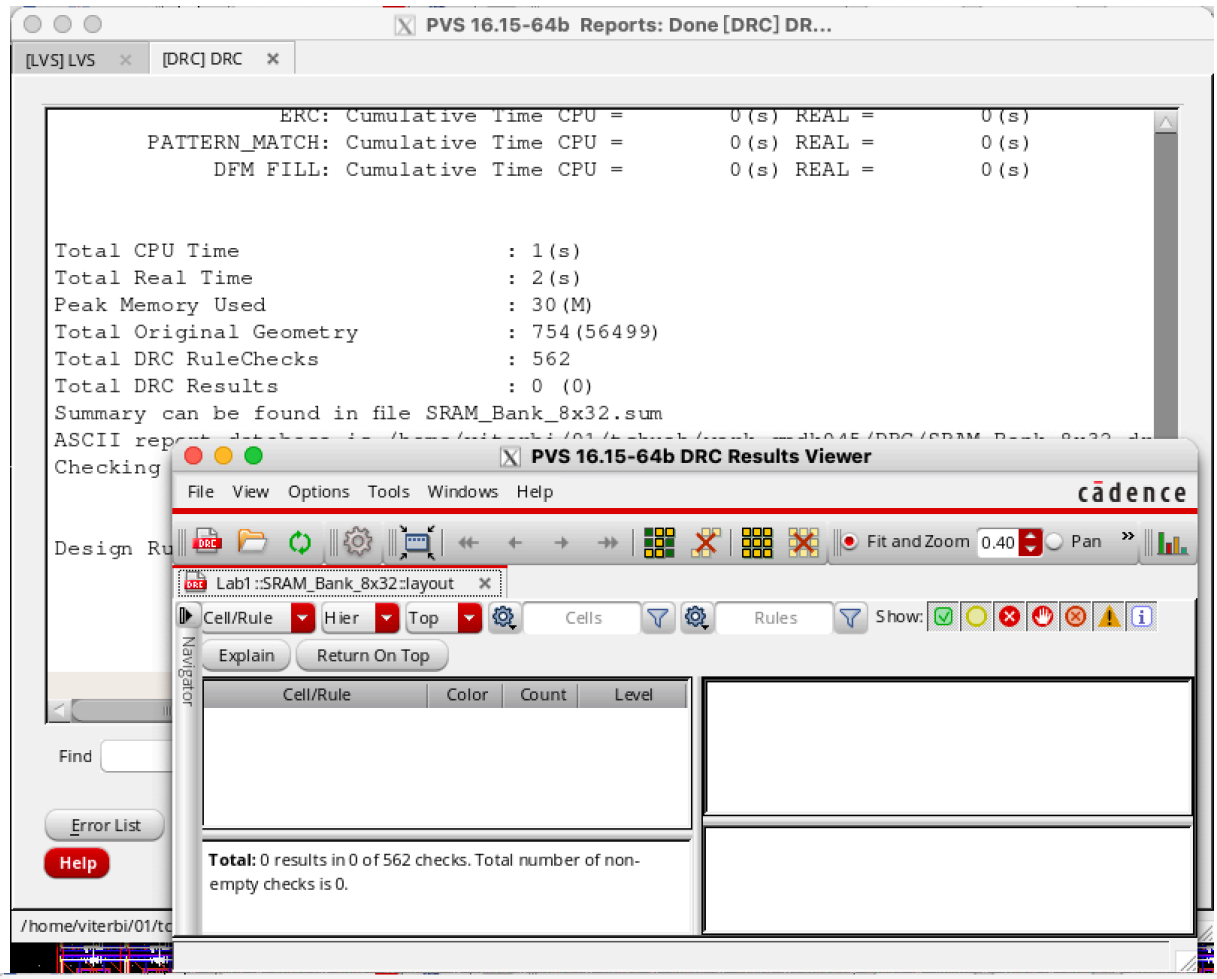


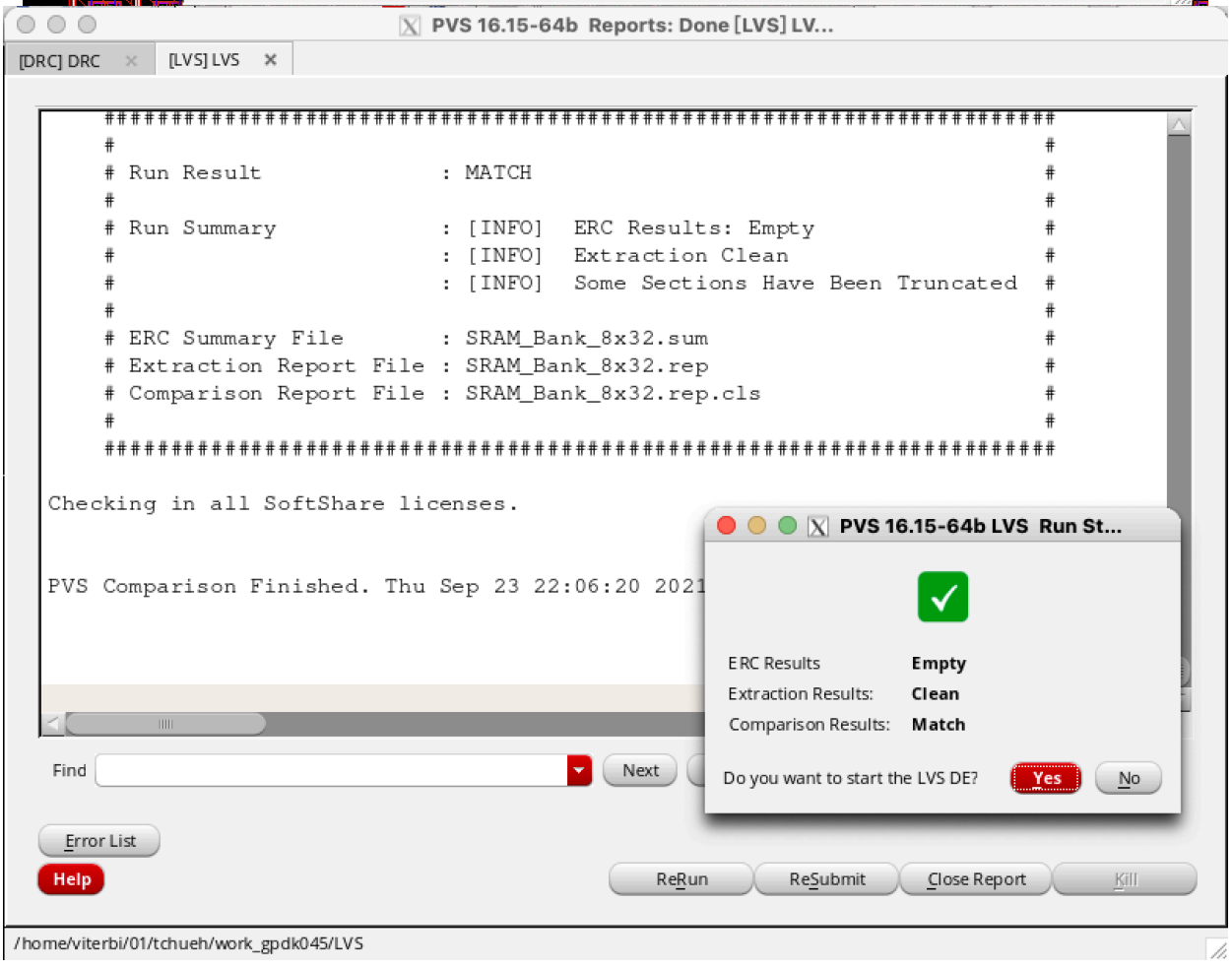
SRAM 8x32 Bank (Layout)



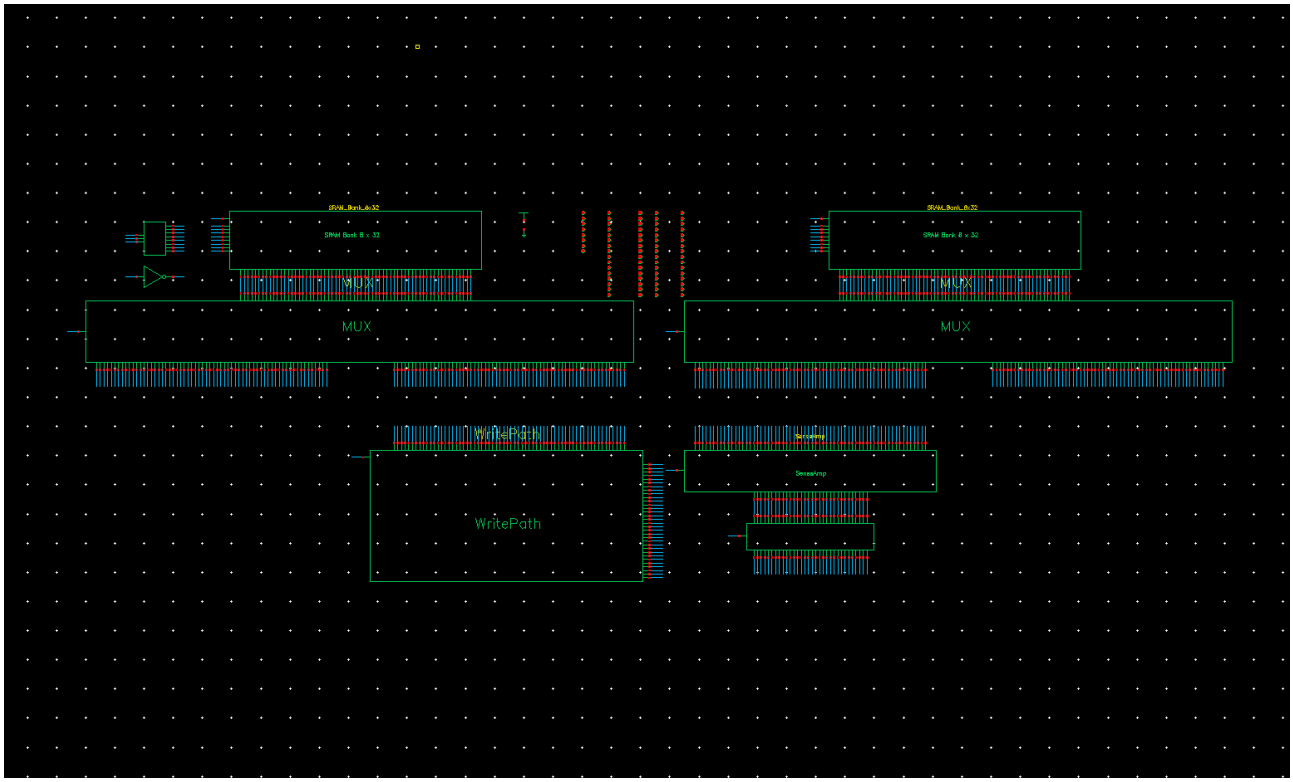
The first row is the pre-charge system and following with 8 SRAM Cells.



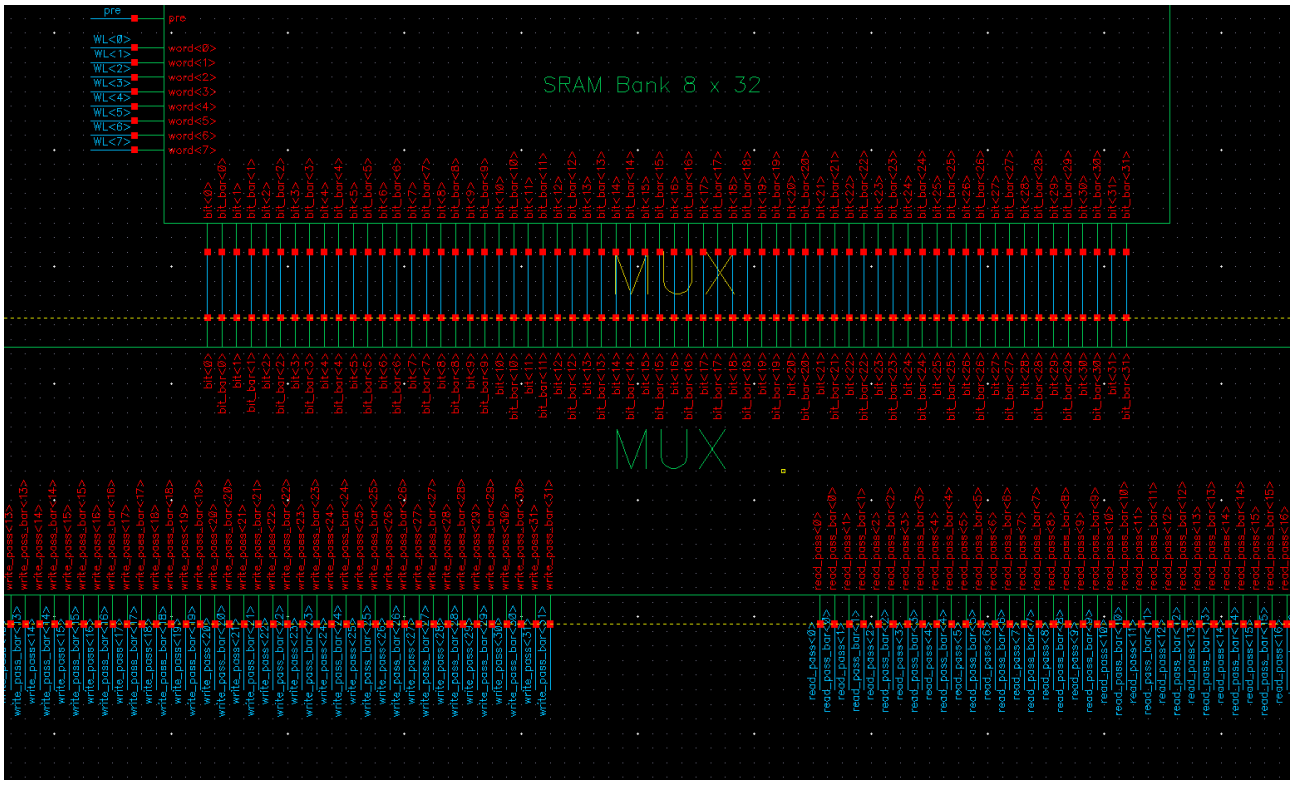

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 2(s)
Peak Memory Used : 30(M)
Total Original Geometry : 754(56499)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file SRAM_Bank_8x32.sum
Checking
Design Ru
Find
Error List
Help
/home/viterbi/01/tc
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1 ::SRAM_Bank_8x32::layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.


PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
: [INFO] Some Sections Have Been Truncated
ERC Summary File : SRAM_Bank_8x32.sum
Extraction Report File : SRAM_Bank_8x32.rep
Comparison Report File : SRAM_Bank_8x32.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 22:06:20 2021
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No

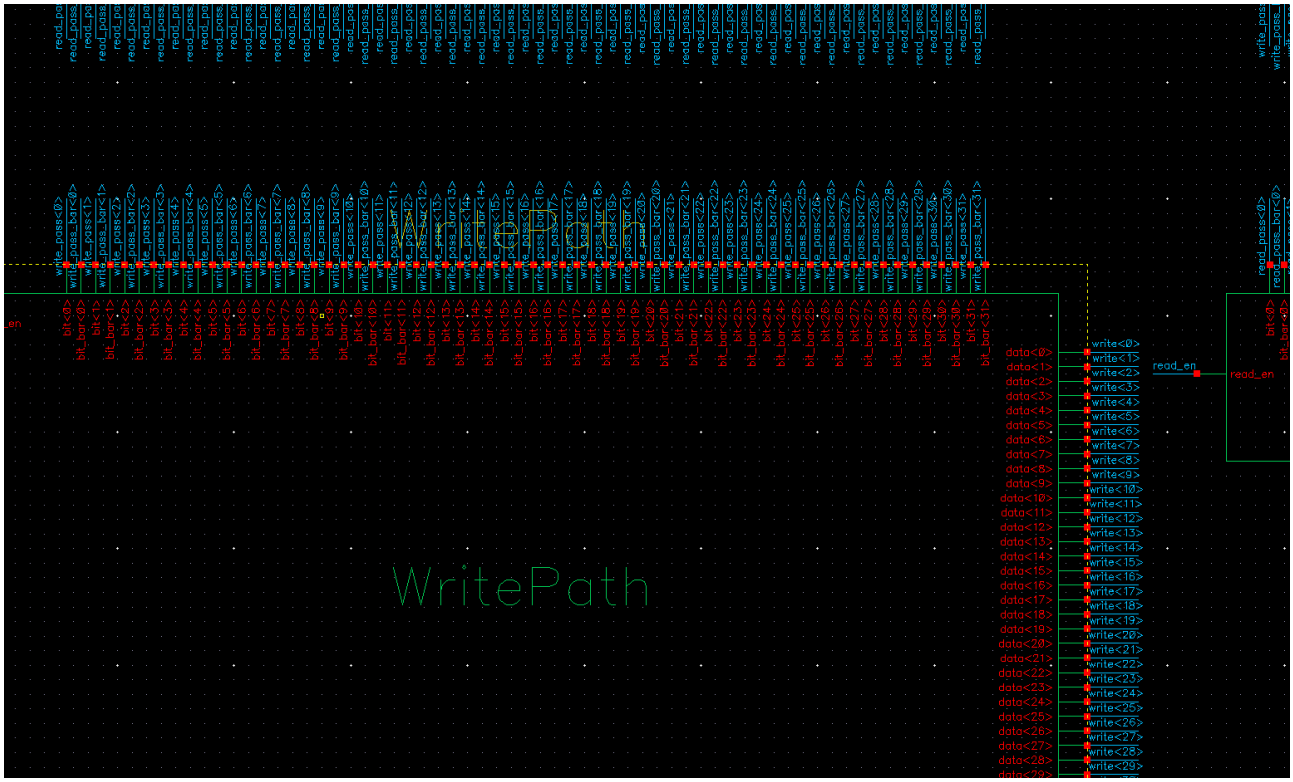
SRAM 512-bit (Schematic)



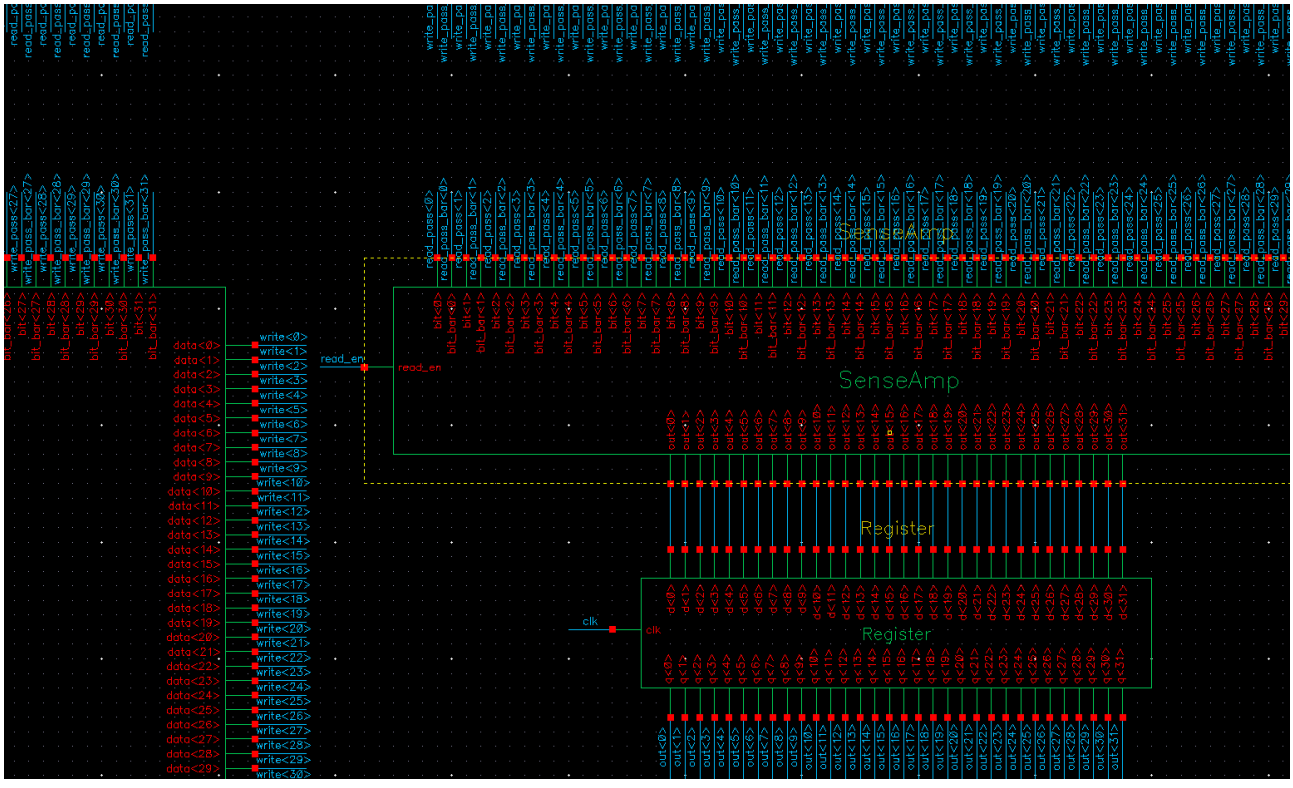
The SRAM Bank is connected to write/read MUX.



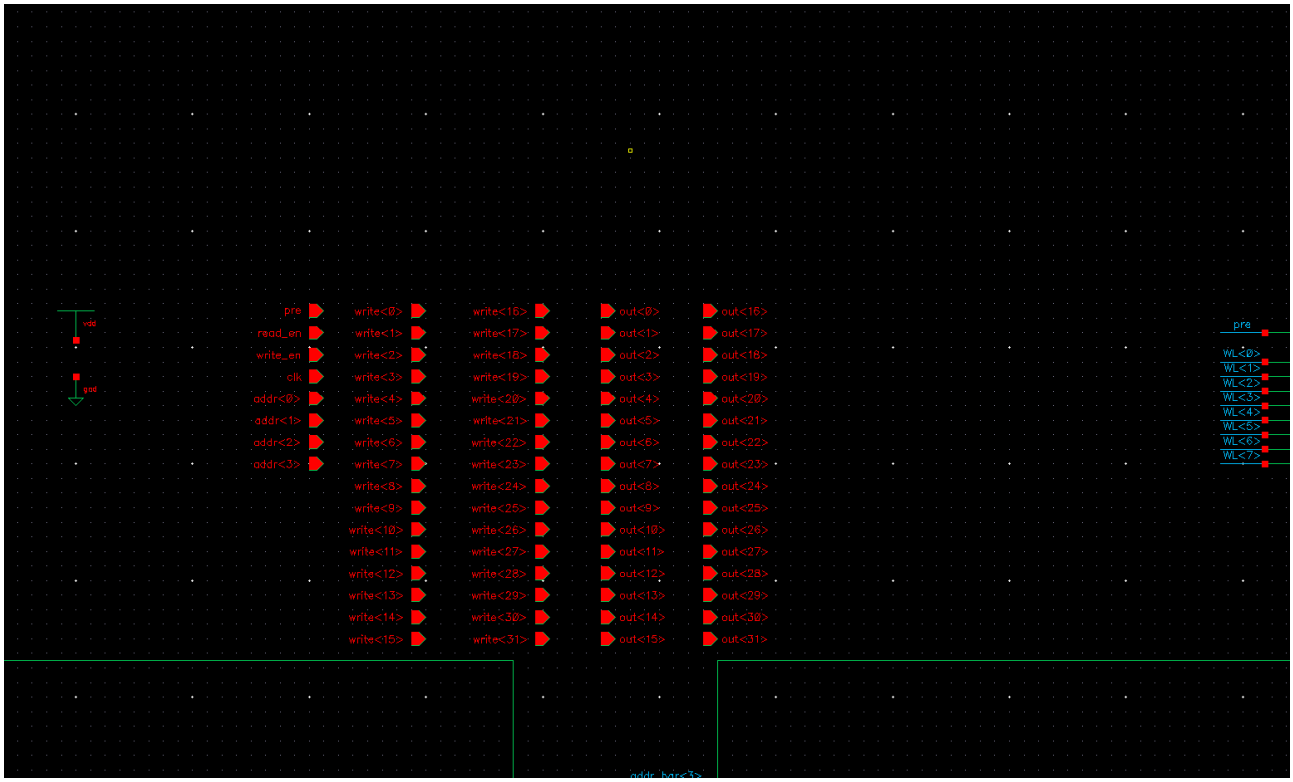
The write_pass of the MUX is connected to the bit line in Write Path.



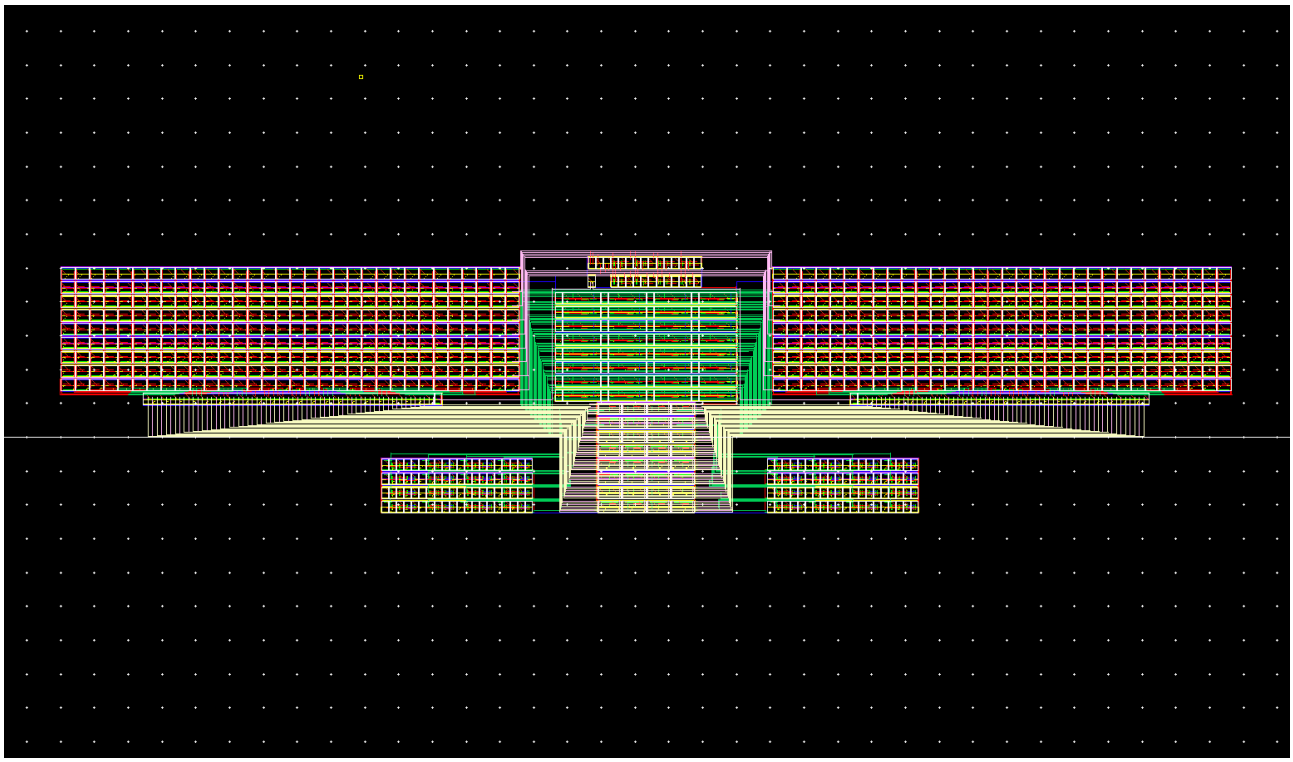
The read_pass of the MUX is connected to the bit line in Sense Amp.

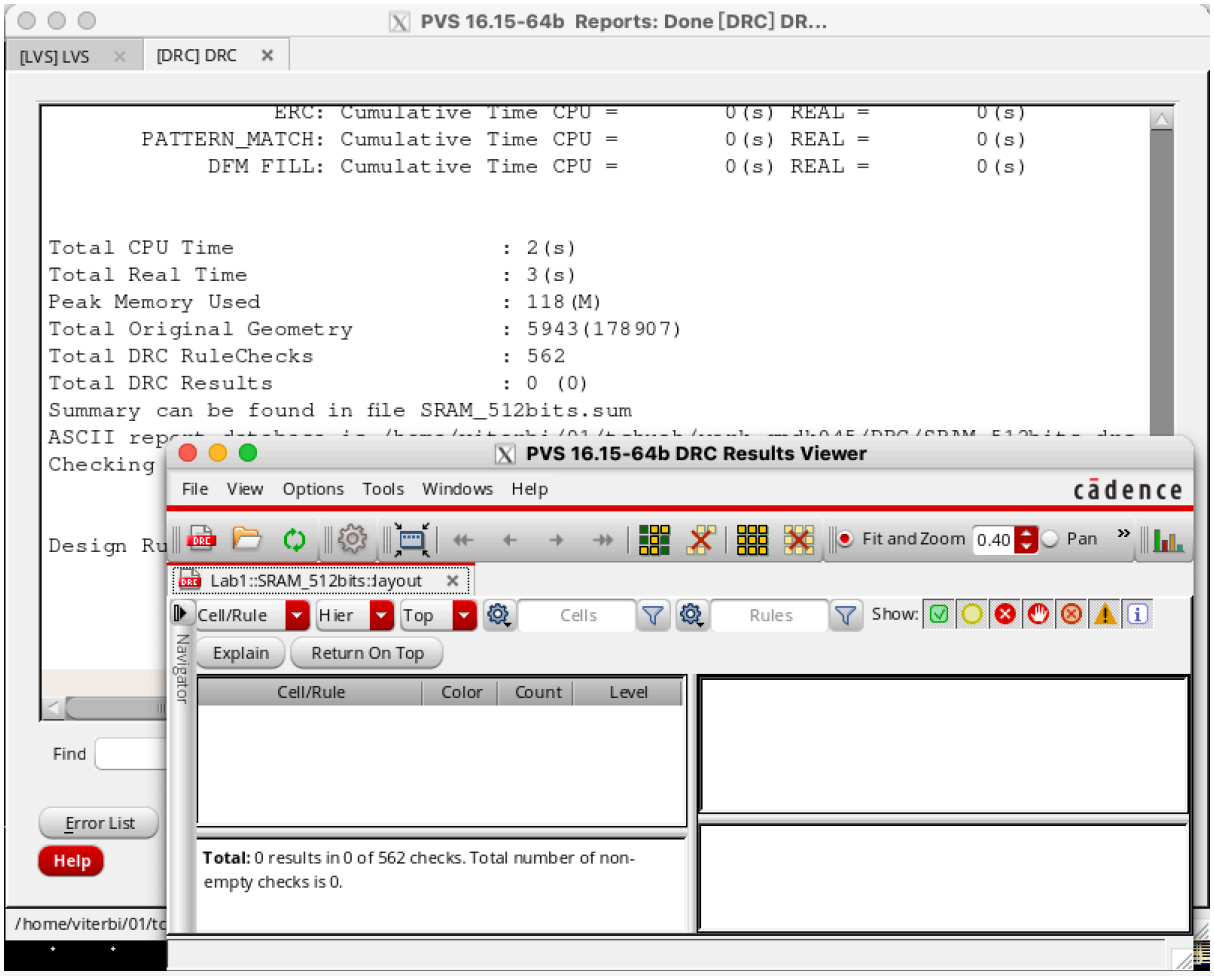


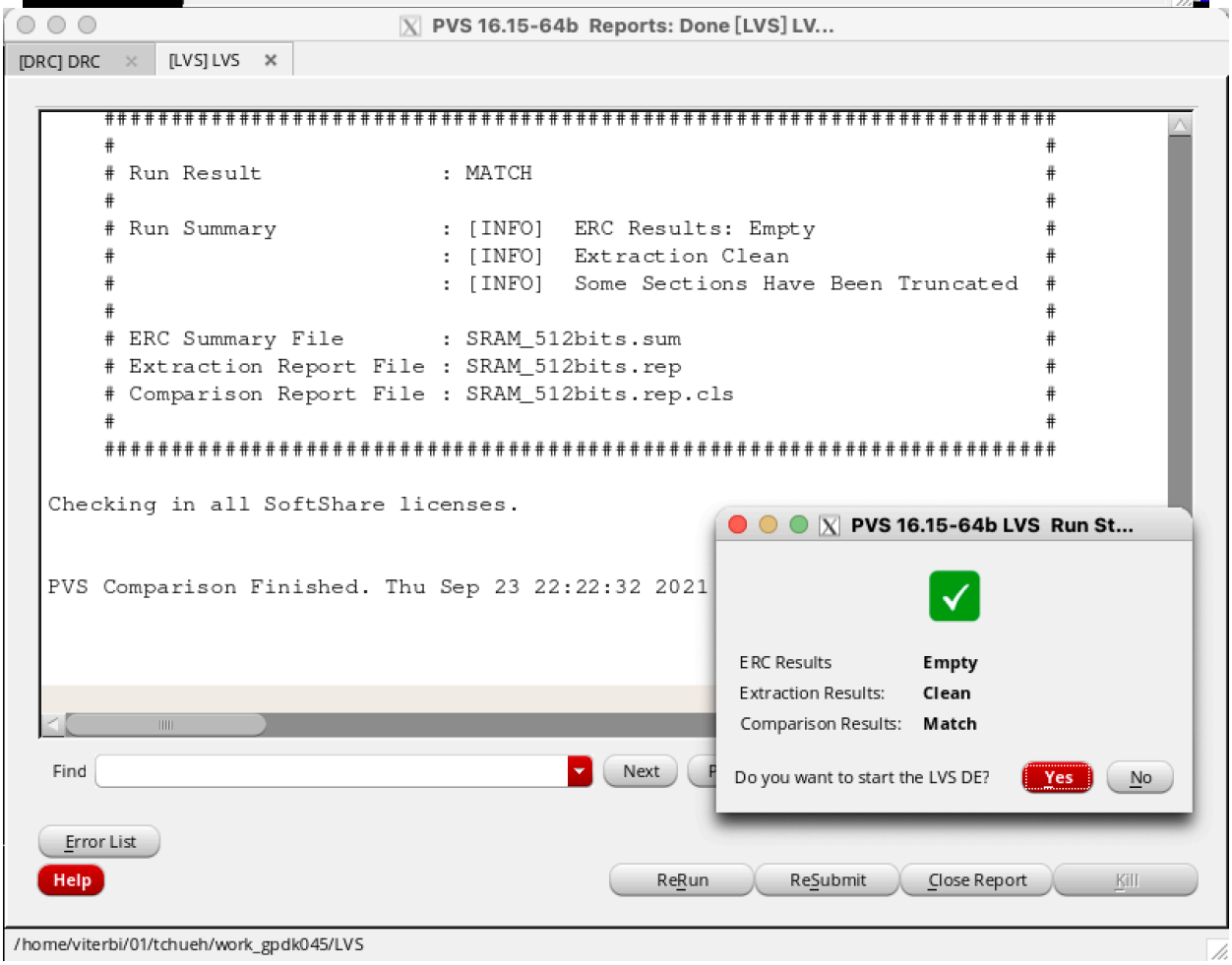
The figure below is the I/O pins of the SRAM 512-bit.



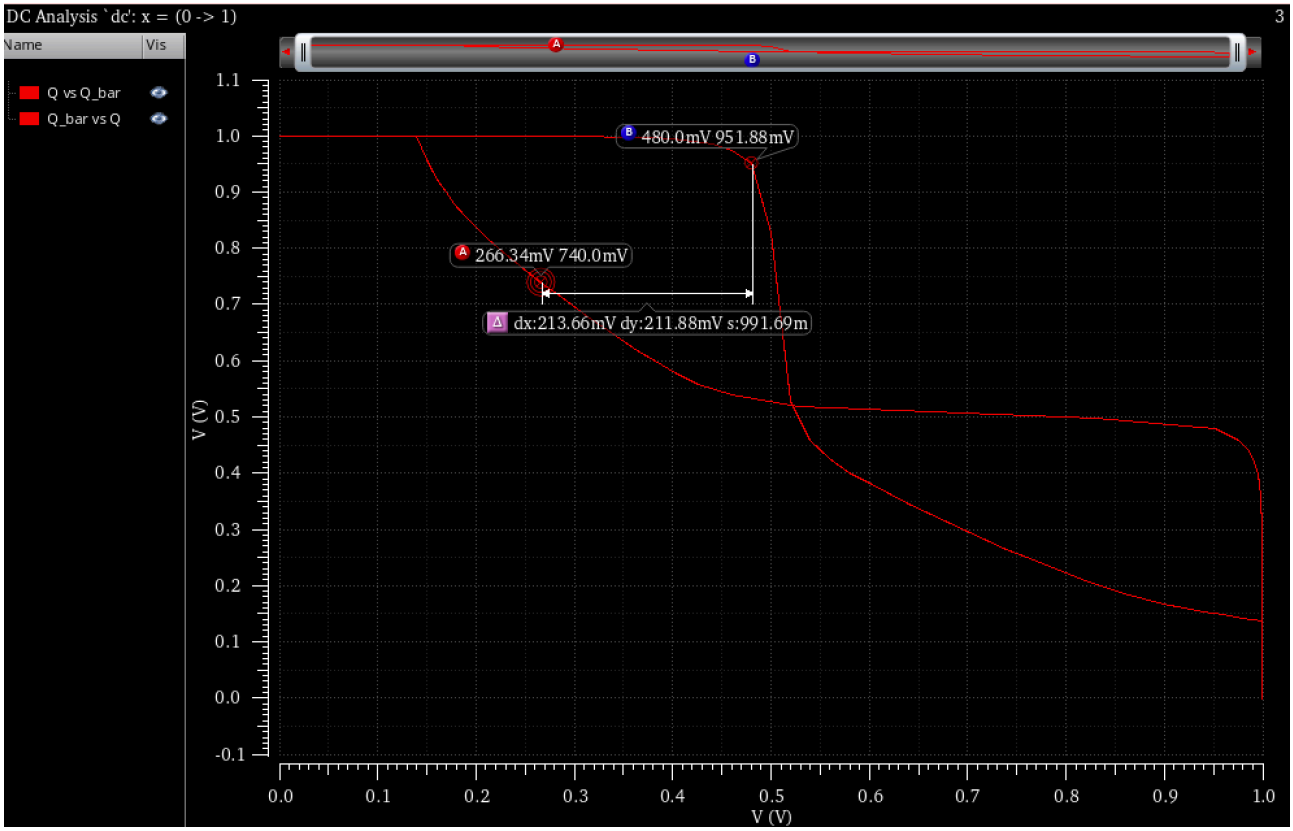
SRAM 512-bit (Layout)



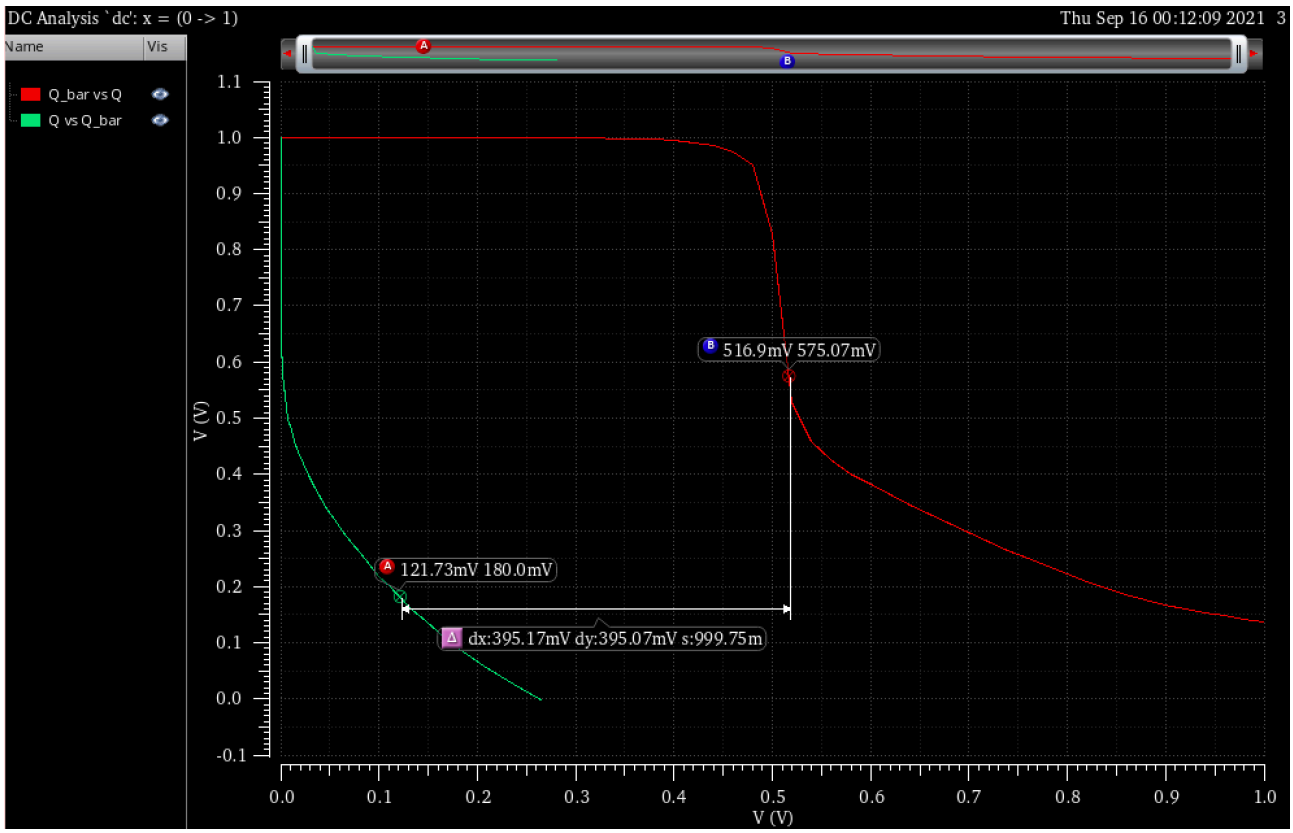

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 2(s)
Total Real Time : 3(s)
Peak Memory Used : 118(M)
Total Original Geometry : 5943(178907)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file SRAM_512bits.sum
Checking
Design Ru
Find
Error List
Help
/home/viterbi/01/tc
PVS 16.15-64b DRC Results Viewer
File View Options Tools Windows Help
cadence
Fit and Zoom 0.40 Pan
Lab1::SRAM_512bits:layout
Cell/Rule Hier Top Cells Rules Show:
Navigator
Explain Return On Top
Cell/Rule Color Count Level
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.


PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
: [INFO] Some Sections Have Been Truncated
ERC Summary File : SRAM_512bits.sum
Extraction Report File : SRAM_512bits.rep
Comparison Report File : SRAM_512bits.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Thu Sep 23 22:22:32 2021
PVS 16.15-64b LVS Run St...
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE? Yes No
Find
Next
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/01/tchueh/work_gpdk045/LVS

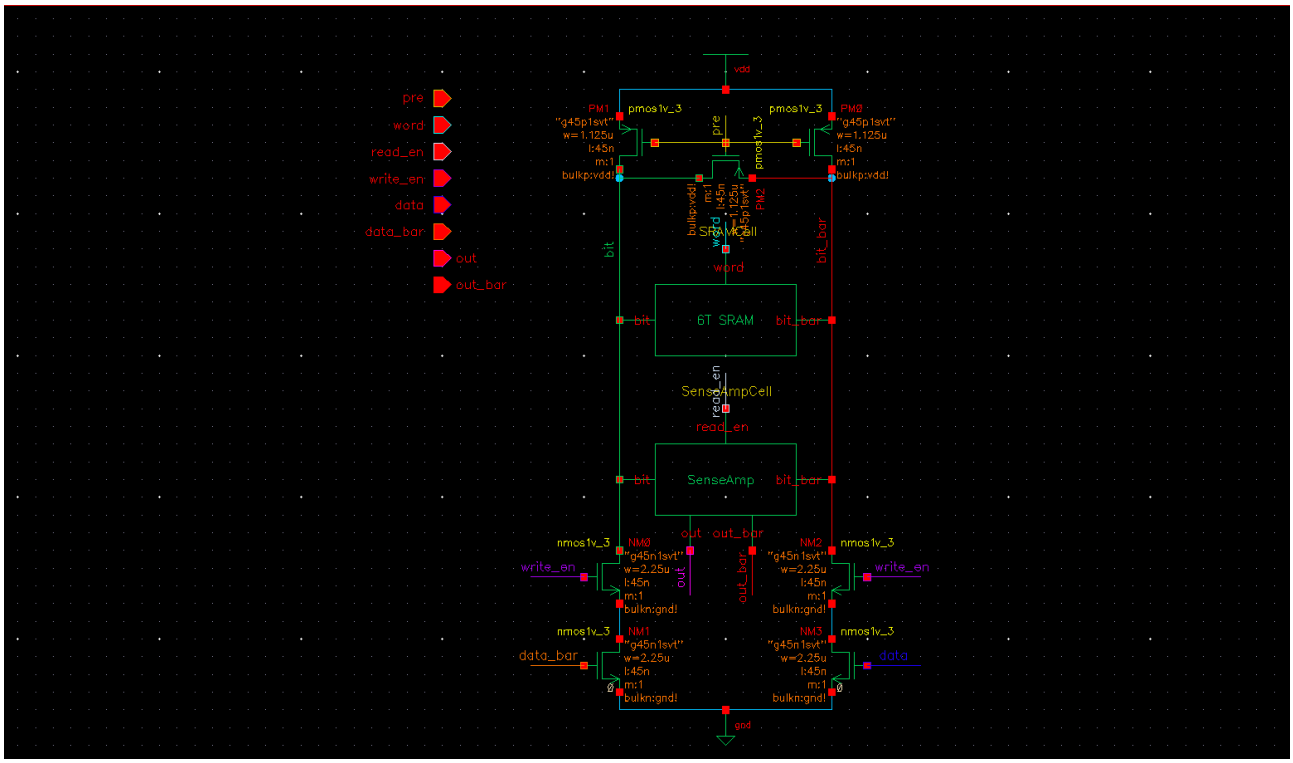
Read SNM is at least 190mV



Write SNM is at least 395mV



SRAM One Cell (Schematic)



The figure below shows the simulation for the single SRAM Cell with the waveform of the operation Write 1→Read→1→Write 0→Read 0.

Write 1	Read 1	Write 0	Read 0
12.57 ps	8.52 ps	11.49 ps	8.52 ps

SRAM operation:

During the write operation, the 32-bit input data will be send to the Write Path. The addr<3> is going decide which Memory Bank will save the data. After that, the output of the Write Path (bit / bit_bar) is pass through the nMOS pass transistors in the MUX and stored in the 256-bit SRAM Bank.

During the read operation, the address we got will decide which word line and which Memory Bank to read from. The Sense Amplifier sense the difference in the bit and bit_bar when the pMOS pass transistors in the MUX tuns on.

Register at the output controls the information when it is available at the clock edge as the Sense Amplifier sense the difference.

Summary:

Area 173.325 x 38.807 = 6726.22328 μm^2

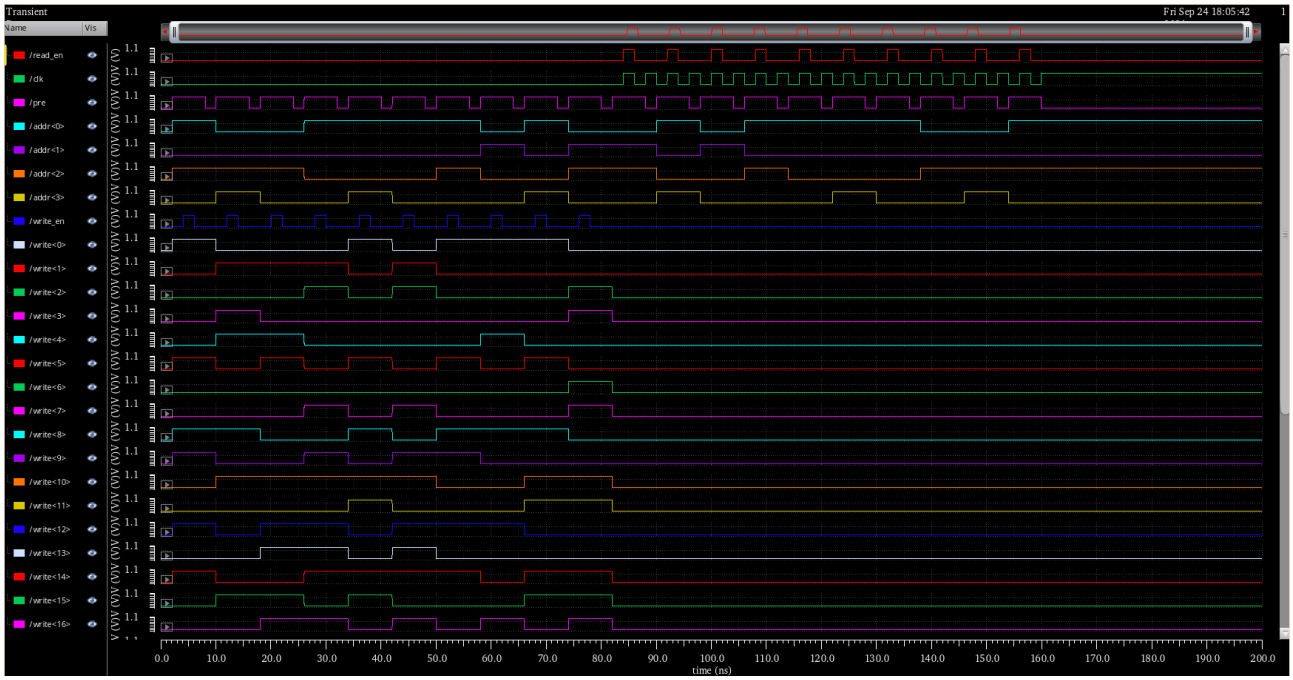
Complete time: 160 ns

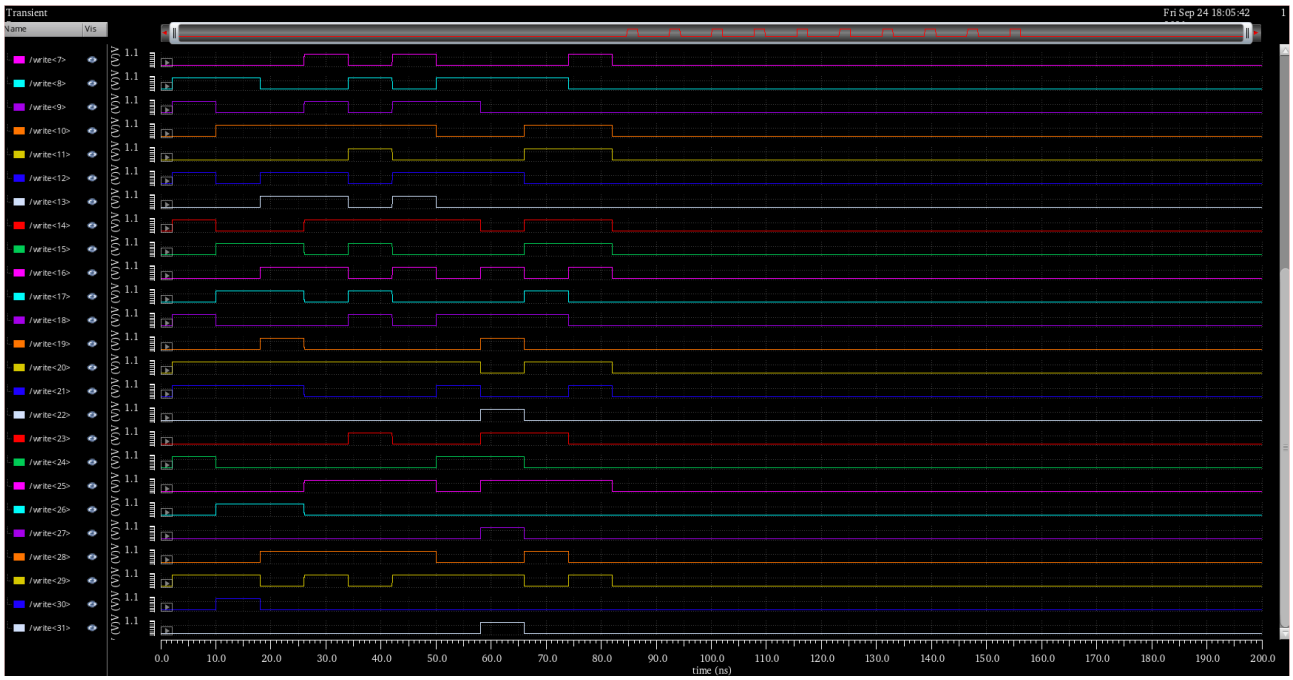
Clock Frequency: 1/4 ns = 250 MHz

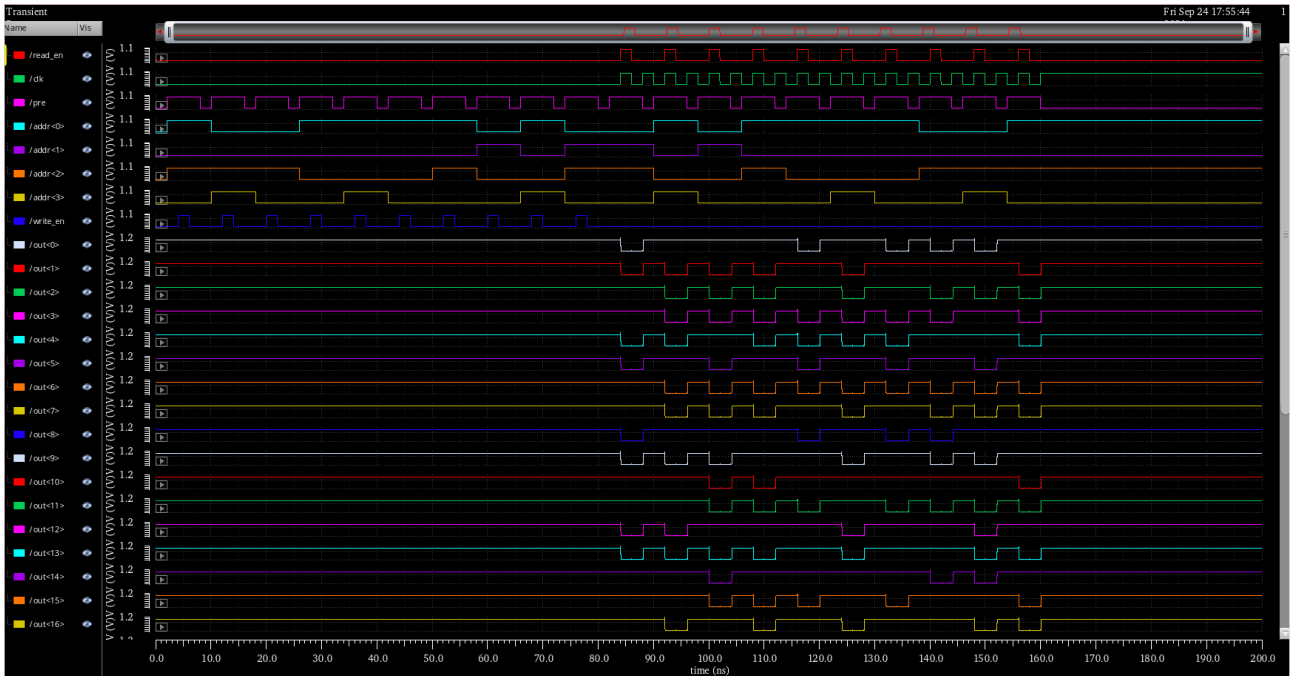
Read 10 data values (32 bit each) from a vector file and write into the SRAM in a sequential order starting from the last digit of your USC ID and then read 10 of them in the sequence of your USC ID.

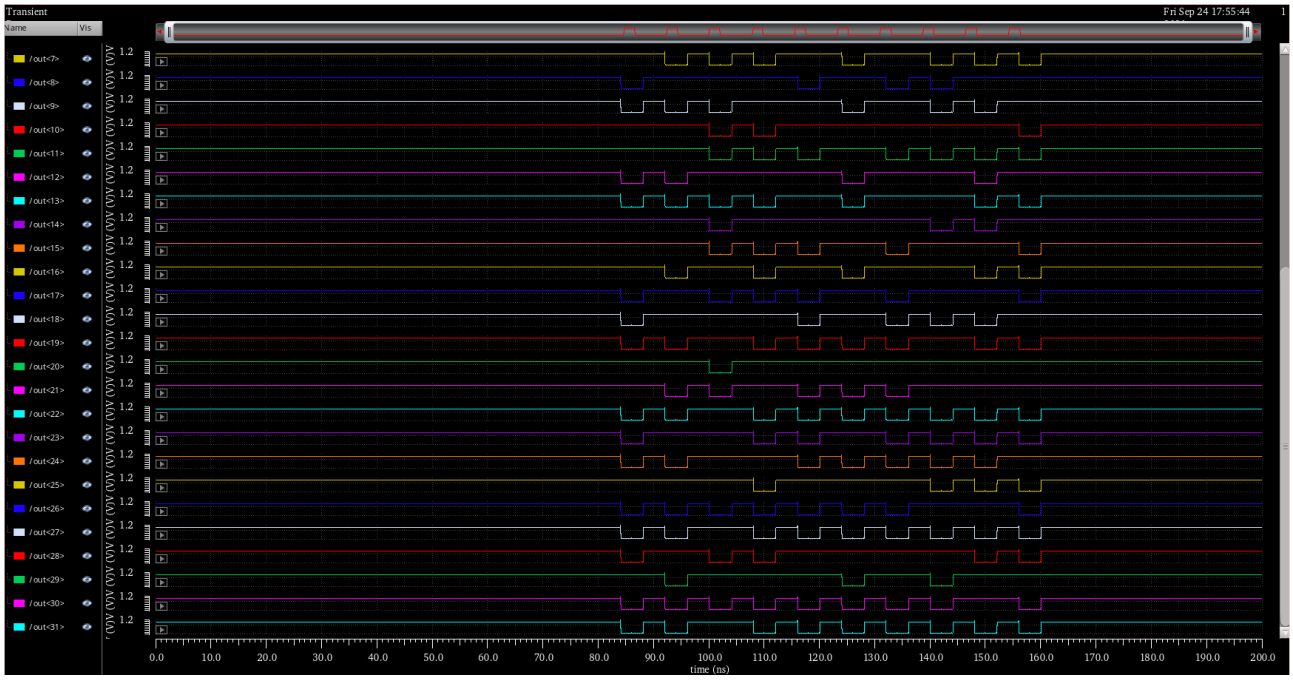
SEQUENCE	A[3]-A[0]	DATA[31]-[0]
0	0100	143B B432
1	0101	2134 5321
2	0111	ABCD 1234
3	0110	2231 CCCC
4	0001	3211 7686
5	0010	ABCD 1111
6	1000	12AB CD91
7	1001	1296 CD21
8	1010	7A5A 6531
9	1100	6432 851A

SRAM 512-bit (Schematic Waveform)

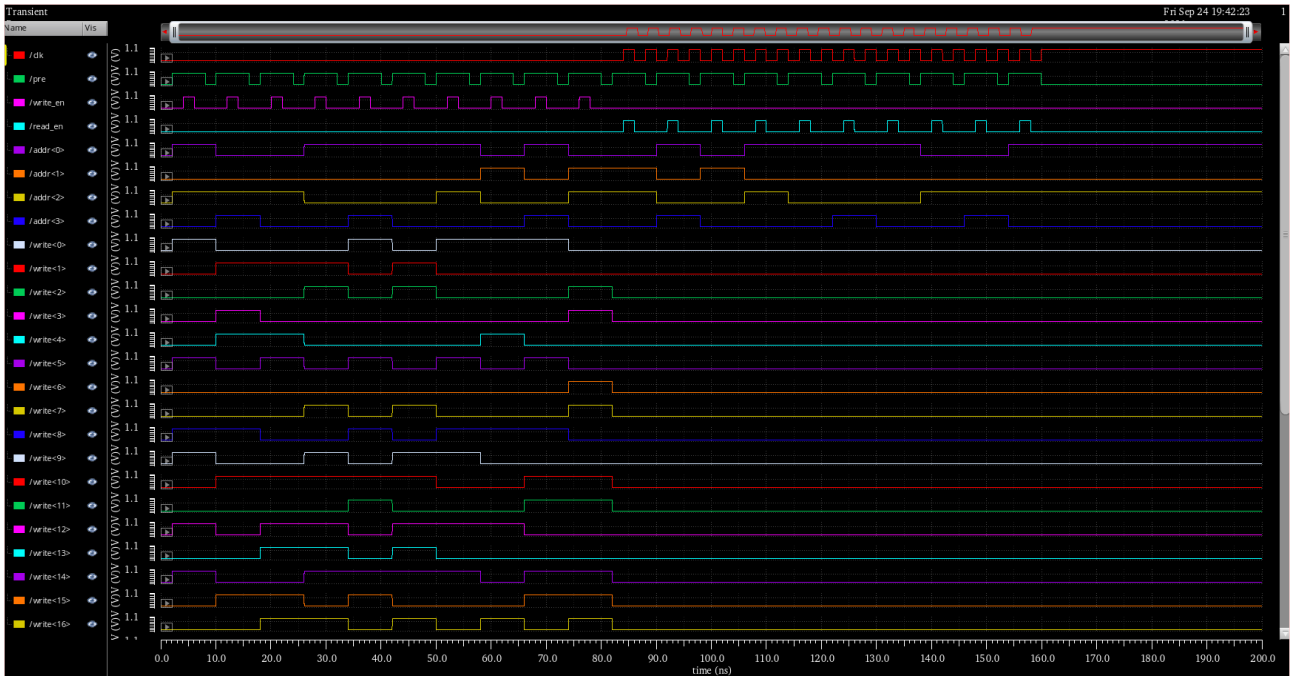


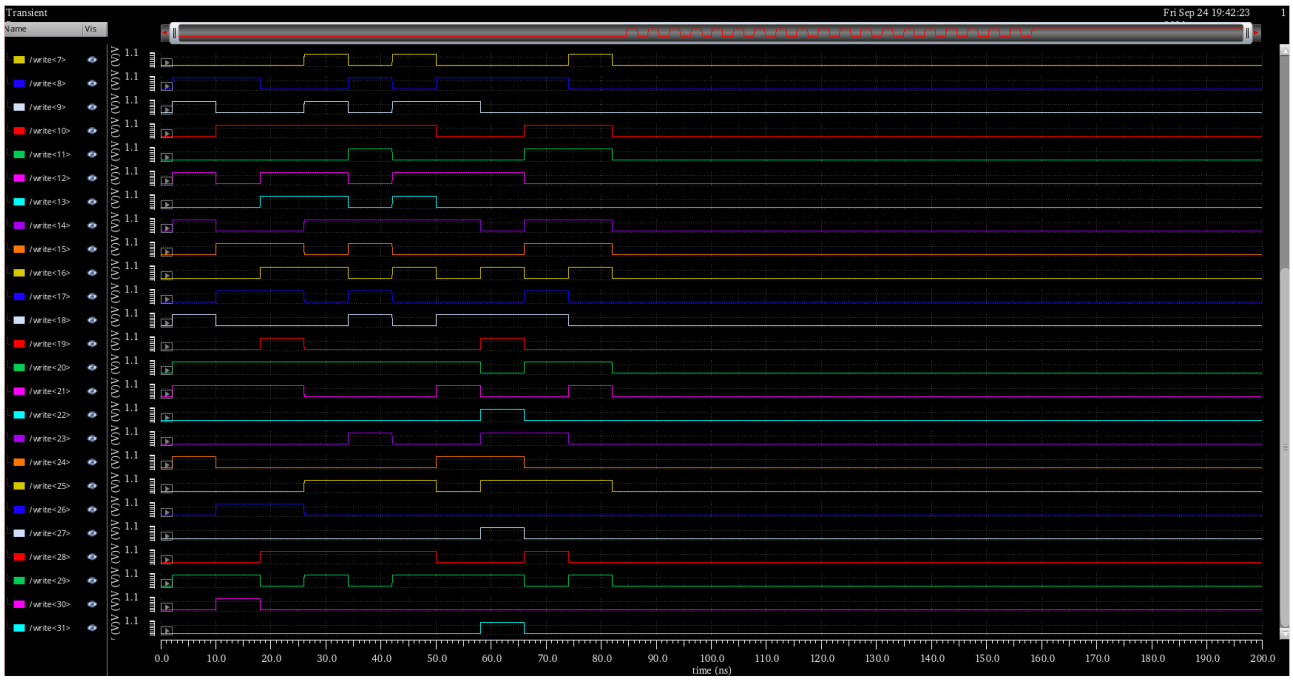


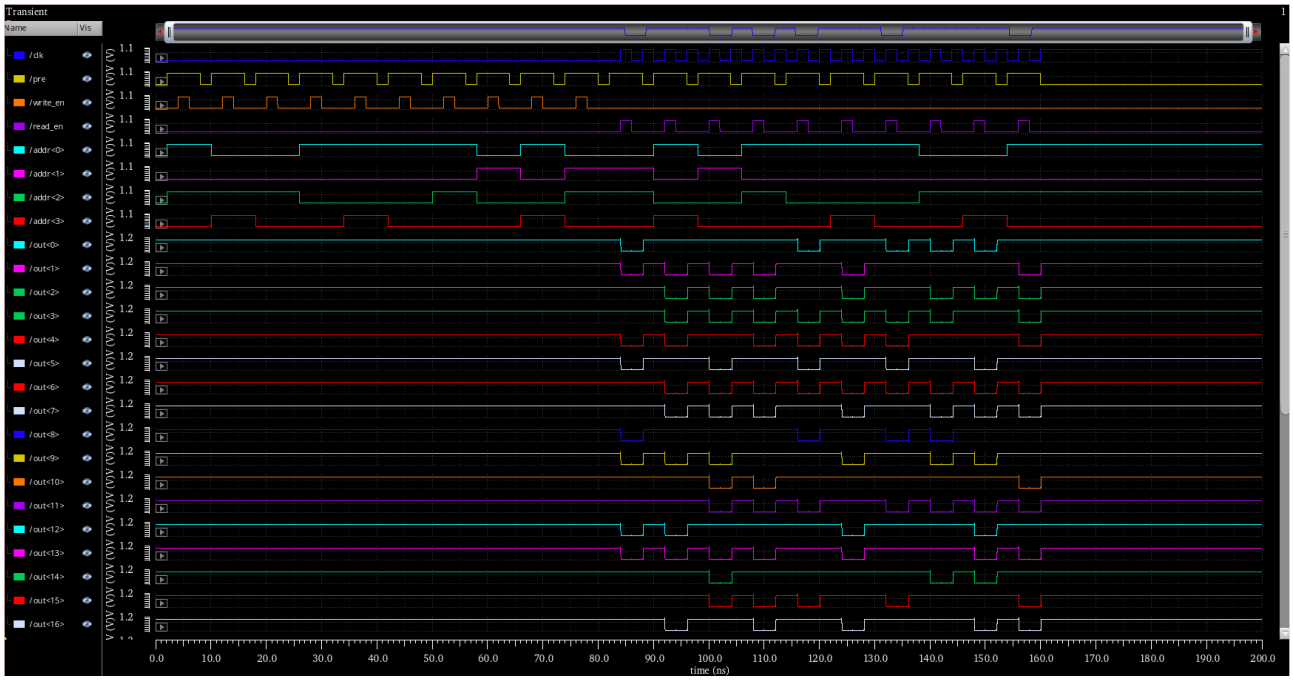

Transient
Fri Sep 24 17:55:44
Name
Vis
/read_en
/clk
/pre
/addr<0>
/addr<1>
/addr<2>
/addr<3>
/write_en
/out<0>
/out<1>
/out<2>
/out<3>
/out<4>
/out<5>
/out<6>
/out<7>
/out<8>
/out<9>
/out<10>
/out<11>
/out<12>
/out<13>
/out<14>
/out<15>
/out<16>
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time (ns)

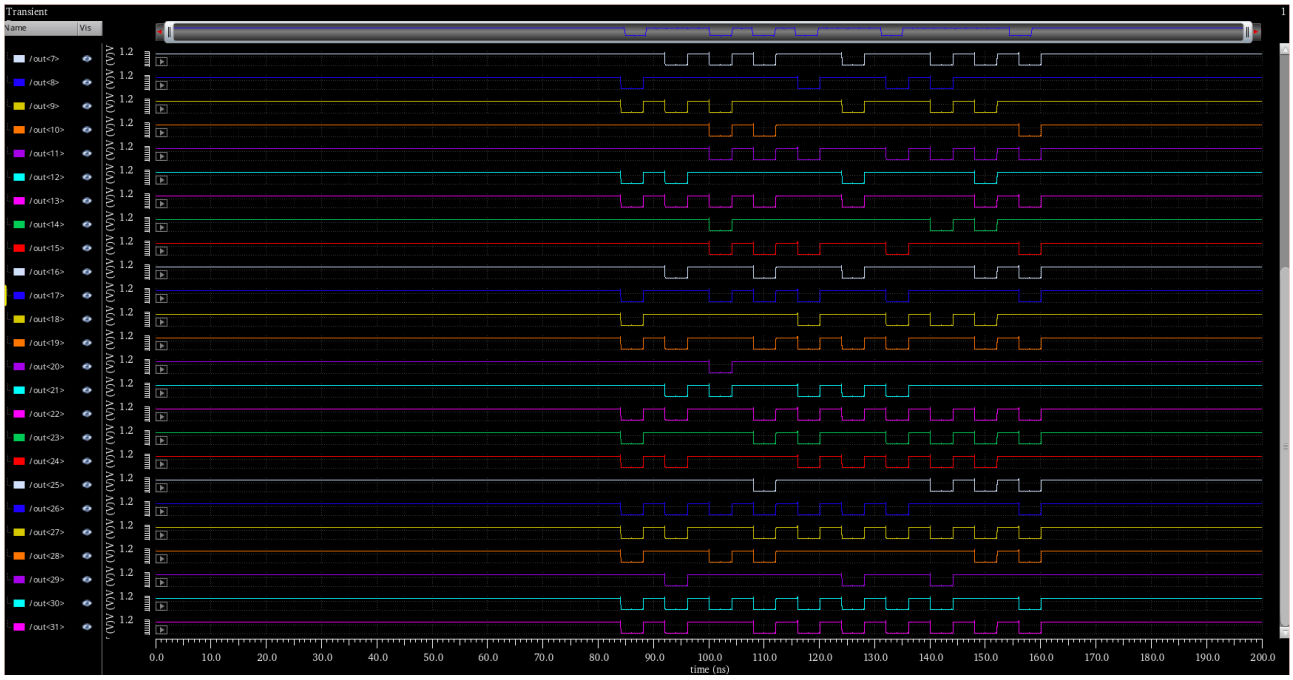

Transient
Fri Sep 24 17:55:44
Name
Vis
/out<7>
/out<8>
/out<9>
/out<10>
/out<11>
/out<12>
/out<13>
/out<14>
/out<15>
/out<16>
/out<17>
/out<18>
/out<19>
/out<20>
/out<21>
/out<22>
/out<23>
/out<24>
/out<25>
/out<26>
/out<27>
/out<28>
/out<29>
/out<30>
/out<31>
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time (ns)

SRAM 512-bit (Extracted Waveform)






Transient
Name
Vis
/clk
/pre
/write_en
/read_en
/addr<0>
/addr<1>
/addr<2>
/addr<3>
/out<0>
/out<1>
/out<2>
/out<3>
/out<4>
/out<5>
/out<6>
/out<7>
/out<8>
/out<9>
/out<10>
/out<11>
/out<12>
/out<13>
/out<14>
/out<15>
/out<16>
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time (ns)


Transient
Name
Vis
/out<7>
/out<8>
/out<9>
/out<10>
/out<11>
/out<12>
/out<13>
/out<14>
/out<15>
/out<16>
/out<17>
/out<18>
/out<19>
/out<20>
/out<21>
/out<22>
/out<23>
/out<24>
/out<25>
/out<26>
/out<27>
/out<28>
/out<29>
/out<30>
/out<31>
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time (ns)