Ti-Shen (Andy), Chueh

Los Angeles, CA | +1 (323) 308-0551 | tchueh@usc.edu | Linkedin: andychueh

EDUCATION

University of Southern California Los Angeles, CA
M.S. in Electrical Engineering *Jan. 2021 - Dec. 2022*
Related Coursework: Computer Systems Architecture, MOS VLSI Circuit & System Design

National Tsing Hua University Hsinchu, Taiwan
B.S. in Engineering and System Science *Sept. 2016 - June 2019*
Related Coursework: Electronics, Electric Circuits, Electronics Lab, Integrated Circuit Design, Programming Languages, Signal and System

EXPERIENCE

Nanoelectronic X-FET Green Devices Lab Hsinchu, Taiwan
Research: N+/P Hybrid Poly-Si Shell Structure Junctionless-FETs *Feb. 2018 - Jan. 2019*
- Outlined the advantages of junctionless field-effect transistors (JL-FETs)
- Presented two types of JL-FETs fabrication (Planar Shell & Nanowire Channel Shell)
- Compared the simulation results with the experiment data
- Exhibited the characteristic of I_D–V_G, I_D–V_D and DIBL
- Analyzed the temperature sensitivity in planar shell & nanowire channel shell JL-FETs

PROJECTS

Digital Logic Design | *Modelsim* *Jan. 2021 - May 2021*
- Completed Single-Clock and Two-Clock FIFO Design
- Implemented simple pipelined system to design 3-Element Adder
- Handled the data dependencies by designing appropriate forwarding unit (FU)

12-bit Multiply-Accumulator (MAC) Unit Design | *Cadence* *Jan. 2021 - May 2021*
- Designed 6x6-bits Wallace Tree multiplier, 16-bit Ripple Carry Adder, and 16-bit D Flip Flop
- Performed the functional verification of the 12-bits Multiply-Accumulator
- Achieved maximum worst-case delay (1.91 ns), maximum achievable clock frequency (101 MHz) and clock period (20896.38 μm^2 * ns)

512-bit SRAM Array Design | *Cadence* *Aug. 2021 - Sept. 2021*
- Designed 512-bit SRAM with two 256-bit Banks (8 x 32), 3-8 Row Decoder, Sense Amplifier, Read / Write Path, Column Multiplexer, and Output Register
- Sized SRAM bit-cell in order to gain better Read / Write Static Noise Margin
- Generated waveforms for consecutive read and write operations
- Summarized maximum achievable clock frequency (250 MHz) and area (6726.22328 μm^2)

CPU Simulation | *SimpleScalar, Cacti , Real Estate Estimation Tool* *Sept. 2021 - Oct. 2021*
- Utilized Cacti to compute the latency of Register Update Unit (RUU) and L1, L2 caches
- Simulated the baseline configuration with the change of fetch/decode/issue/commit width
- Compared the MIPS, total area, and total transistor count in different machine width

TECHNICAL SKILLS

Programming: Java, C++, Matlab, Verilog RTL, MySQL, VHDL, HTML
Developer Tools: Cadence, Modelsim, VirtualBox, SimpleScalar, Cacti